Although the words "he," "him," and "his" are used sparingly in this manual to enhance communication, they are not intended to be gender driven nor to affront or discriminate against anyone reading *Ocean Systems Technician 3 & 2 (Maintainer)*, Module 4, NAVEDTRA 062-04-45-85.

Naval Education And Training Program Developmen

OCEAN SYSTEMS TECHNICIAN 3 (MAINTAINER)

MODULE 4

OCEAN SYSTEMS COMPUTERS, PROCESSO AND PERIPHERAL EQUIPMENT

NAVEDTRA 062-04-45-85

1985 Edition Prepared by
OTMC Roy M. Derrick

PREFACE

This Rate Training Module and Nonresident Career Course (NRCC) form a self-study package that will enable Ocean Systems Technicians to help themselves fulfill the requirements of their rating.

This Module is part of a series written for personnel who are specializing in the maintenance aspects of the Ocean Systems Technician (OT) rating.

Designed for individual study and not formal classroom instruction, this Module provides subject matter that relates directly to the occupational standards of the OT rating. The NRCC provides a way of satisfying the requirements for completing the Module. The assignments in the NRCC include learning objectives and supporting questions designed to lead the student through the Module.

Special appreciation is expressed to Commander, Oceanographic System Atlantic, Commander, Oceanographic System Pacific, and the Fleet ASW Training Center Atlantic, for their contributions to the development of this module.

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THE UNITED STATES NAVY

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The United States Navy is responsible for maintaining control of t
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It is upon the maintenance of this control that our country's glorio
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under the sea, and in the air.

Now and in the future, control of the sea gives the United States
greatest advantage for the maintenance of peace and for victory
war.

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CREDITS

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SOURCE	ILLUSTRATIONS
Beehive International	Figures 3-3 through 3-10 and Table 3-1
GENICOM Corp.	Figures 3-11 through 3-15, 3-18, and 3-20
McGraw-Hill	Figures 1-8 through 1-48, 1-50, 1-51, and Table 1-2

The Rate Training Manual for the Ocean Systems Technician 3 & 2 rating is developed in modular format by occupational speciality. The following list provides an outline of module contents and approximate distribution dates.

ANALYST

Module 1—The OT Rating, NAVEDTRA 052-01-45-83

This module reviews the career paths available to "OT" personnel and security regulations applicable to the rating. Currently available.

Module 2—Physics of Sound, NAVEDTRA 052-02-45-81

This module provides information about sound travel through water and its effect on Lofar detections. Currently available.

Module 3—Analysis, NAVEDTRA 052-03-45-81

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This module will provide information on the operational characteristics of the various Oceanographic subsystems. Availability to be announced.

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This module reviews the career paths available to "OT" personnel and security regulations applicable to the rating. Currently available.

Module 2—General Maintenance, NAVEDTRA 062-02-45-82

This module provides information on the use of publications, station drawings, and schematics, modular construction and soldering. Currently available.

Module 3—Equipment Maintenance, NAVEDTRA 062-03-45-82

This module provides information on the various AN/FQQ front ends, a walk through of a typical system, special purpose test equipment, Recorder/Reproducer AN/USH-3(V)2, and PMS. Currently available.

Module 4—Ocean Systems Computers, Processors, and Peripheral Equipment, NAVEDTRA 062-04-45-85

This module provides information on the technical and operational characteristics

PART 1

INTRODUCTION TO COMPUTERS

Before you learn about modern-day com- uters, it is useful to know of the historical evelopment of these devices. Modern computing evices are the result of centuries of development rom ancient man to the present state-of-the-art echnologies. Only by learning of this develop- nent can the present technologies be fully under- ood and appreciated and avenues for further efinement provided. Upon completion of this opic you will be able to describe the historical evelopment of the computer, its applications, the ypes of devices in use today, and the electronic ements used in these machines. An introduction computer programming concepts is provided you can identify the procedures used in the reparation of a computer program. A glossary f commonly used computer terminology is also rovided.

HISTORICAL DEVELOPMENTS

History indicates that computing devices and heir associated numbering systems have devel- ped along similar lines. In fact, the computing evices available may have caused the develop- nent of a numbering system. Early man used his ngers to count (a practice still widely followed). y assigning one item to each digit he could keep ack of his possessions. For the fortunate indi- iduals whose possessions exceeded the count of n, stones or pebbles were probably used in the ccounting process. A quick comparison of pos- essions and the accounting system would identify

Most early languages contained wordin or two items but rarely for many. With opment of new names for numbering modern counting and numbering syst also developed. Perhaps a different colo of stone would represent a certain v example, five, ten, and so forth. Mone tems are an outgrowth of this idea.

The complexity of these systems, which used a special symbol or combi symbols, was perhaps a major fac inhibited scientific development. In ab A.D. the presently used Hindu-Arabic counting and mathematical manipulatio its final stage of evolution. This syst simplified mathematical calculations longer required mathematicians to solv tary problems.

RECENT DEVELOPMENTS

Simplified computations did not imn lead to rapid advances in science. In fact, until about 1600 A.D. that the socioe conditions of the times improved to t where any real scientific progress could With the invention of Napier's Bones (which used the newly developed co logarithms), man began to devise and de a rapidly increasing rate, complex device with his computations. Prior to this abacus (figure 1-1), a static storage d the progressive results of decimal calculation, was one of the few aids available to man. The abacus consists of a rectangular frame with a crossbar supporting a number of parallel wires. Each wire contains a number of beads which are free to slide on the wires. Above the crossbar there is normally one or two beads, each worth five units; below the crossbar there is normally four or five beads, each worth one unit. Although the abacus originated in China, its use spread to many parts of the world and, even today, it is widely used in many countries.

Blaise Pascal, a Frenchman, developed a type of adding machine in 1642. This early forerunner of a desk-top calculator was completely mechanical and could perform addition and subtraction. It incorporated an automatic carry and borrow function which made it more advanced than other devices then in existence.

In 1820, John Thomas, also a Frenchman, took a somewhat unreliable machine designed by a German mathematician and by improving it made a commercially successful calculator capable of multiplication and division.

In 1822, an English mathematician, Charles Babbage developed a calculator to solve algebra equations. His device, called a difference engine could calculate the values for Y in a quadratic equation when given the first and second differences. The principle of construction for the machine was based on the investigations of the German mathematician Muller in 1786. Babbage's chief problem in the development of this and later models was the lack of technology to construct the intricate mechanical parts. Assisted by the English government, Babbage produced a working model of his engine but failed to complete a full-scale working model. The technology to produce the machine had to be developed along with the device. This forced Babbage to drop the project in 1833.

The "analytical engine," a mechanical forerunner of the modern computer, was under

engineering, drawing, and acc
are industrial standards even

In developing the analytica
used punched cards to feed in
machine. This concept is still u
computers. This technique o
French inventer Joseph Marie J
into pattern weaving in the Fre
Jacquard's method of "progr
looms involved a language wi
hole or no hole. A close parall
today's computers which use

Herman Hollerith, an An
machines that could evaluate
punched cards. The card code
developed to solve problems f
of Census. The U.S. populati
1890 that if existing techniqu
would have taken 12 years t
Hollerith's methods and mac
data in about 2 years. His de
first electromechanical device
company that produced Holl
now part of the IBM Corpo

Another electromechanic
about 1914 with the introdu
card machine called a vertical
was replaced 13 years later wi
like those in use today with h
the printing card sorter.

A department store in Pe
first sales recorder installed
recorder connected by wire to
facility.

The zenith for mechanical
in 1930 in the form of a "dif
This machine was used to cal
of artillery shells in World

The progress during the 1
a number of relay-type compu
Dr. Howard Aiken concei
automatic data processing sy
system was known as the A
Controlled Calculator or

Table 1-1.—Evolutionary Developments in ADP

DATE	WHO	WHAT
4000 - 3000 B. C.	Chinese	ABACUS–Mechanical predecesso day digital computers
1300 A. D.	HINDUS and ARABIANS	Final evolution of modern numbe ulation systems (adding - subtracti multiplying and dividing)
1617	Napier	NAPIER'S BONES–Mechanical d logarithms
1630	Oughtred	SLIDE RULE–Mechanical device logarithms and antilogarithms per rapid calculations (the first analog
1642	Pascal	MECHANICAL ADDING MACHI driven wheel device (capable of pe both addition and subtraction)
1671	Leibniz	CALCULATING MACHINE–Ste device (capable of addition - subtr multiplication and division)
1804	Jacquard	PUNCHED CARDS–System for c weaver's loom–predecessor of mo punched card accounting system
1820	Thomas of Alsac	ARITHMOMETER–first practical wheel commercial calculator
1822	Charles Babbage	"DIFFERENCE ENGINE"–Conc model of device which was intend up tables of mathematical functio their successive difference
1830 - early 1900's	C. Babbage and his son H. P. Babbage	"ANALYTICAL ENGINE"–Conc which was intended to perform an sequence of calculations and have store numbers, print results, go ba

Table 1-1.—Evolutionary Developments in ADP—Continued

DATE	WHO	WHAT
1872	Baldwin	CALCULATOR—Invented pinv counter control
1886	Felt	The Felt "Macaroni" box—the order key driven calculator—a f of the comptometer
1890	Hollerith	PUNCHED CARD CODE and s for sorting and counting punch founded corporation that begar

The first electronic computer was the Electronic Numerical Integrator and Computer (ENIAC). Work on ENIAC was started in 1939 at the University of Pennsylvania's Moore School of Electrical Engineering by a group under the direction of J. P. Eckert, an engineer, and J. W. Mauchly, a mathematician. ENIAC, when completed in 1946, used about 1,500 relays and 18,000 vacuum tubes and could complete an addition sequence in about 1/300th the time required by the Harvard Mark I.

ENIAC had several disadvantages, however, which severely restricted its use, among which were a limited storage capacity and the difficulty of presenting instructions. Instead of correcting the deficiencies of ENIAC, Eckert, Mauchly, and associates immediately began work on a new machine. This new machine, which was known as the Electronic Discrete Variable Automatic Calculator (EDVAC), was a stored-program type of computer. It used an acoustic-delay storage device that greatly increased its storage

During the 1940s many
computers were constructed.
the IBM Selective Sequence El
the Harvard Mark III, ar
Standards Eastern Automatic
After EDVAC, Eckert and
business for themselves.

The first commercially
was the Universal Au
(UNIVAC). It was originally
Eckert, Mauchly Corporati
U.S. Bureau of Census.

The original UNIVAC w
computer built to handle bo
numerical data. It had a c
million pulses per second, a
storage or memory that use
system, and ten servo units fo
tape inputs and outputs. It
high-speed printer as an ou
improvements have been ma
duction of the original U
computers of today are

eywell, Datamatics, and the UNIVAC ion of Sperry-Rand.

handy reference table defining the evolu- from the first crude computing methods to lectromechanical devices of the 1800s and 1900s is contained in table 1-1.

COMPUTER MAKEUP

he electronic components of a computer odes ray tubes, transistors, microchips, ed circuit cards, and so on) are commonly d hardware. Software, on the other hand, is m which is applied to a set of computer rams, procedures and, possibly, associated mentation concerned with the operation of ta processing system. Software includes bilers, assemblers, executional routines, and /output libraries. The advances in computer vare provide the industry with the greatest n of application possibilities. The problem tempting to communicate with a computer ed to the development of symbolic languages approach human language. The fact that a on can tell a computer what to do, just as directs the actions of another person, has made possible by the advances in software. rogramming in a universal language has led e development and refinement of a number mputer languages. Many of these languages or a special area or purpose; for example, TRAN (FORmula TRANslator) for business scientific programs, COBOL (COmmon ness Oriented Language) for business and l for large scale, computer-based, command control systems. PL/1 (Programming uage/one) is a language for real-time ms. Each of the languages fulfills a specific for a specific problem but lacks the universal application.

oftware is also used to overcome design iencies in computers. Programming around

airline reservations system where the cler immediate access to information, the abil manipulate this information, and restorin altered information in the computer memc other mass-storage facilities.

COMPUTER APPLICATIONS

Computer applications fall into a varie broad categories. Information retrieval is such application or in a narrower sense ind or cataloging. Information is stored unc variety of key words or index headings. By c up one of these headings, a listing of all or of the information will be output by the comp Another application is simulation. This inv simulating the operation of a new com using an older computer model. In this design deficiencies can be identified wi going through the time-consuming and expe process of building the newer unit. Real control of a production process is another a cation. For example, the petroleum and che industries put this process to good use. computer can detect minute changes in production process and initiate immediate rective action.

The advent of personal (home) comp has greatly expanded the computer-use hor from the routine upkeep of a checkbook ba to the more complex functions of fina planning, home security, and computer games. The application of the computer an functions is virtually endless. For this re there are some people who believe tha computer will soon control everything everyone. This is not necessarily the however, computers can do only what creators have intended them to do. The com enables man to do more than he has able to do before. For example, computa new skill (a laborer may have to be retrained as a computer programmer or machine operator). Rather than destroying jobs, the computer creates opportunities where none existed before.

TYPES OF COMPUTERS

In general, there are two basic types of computers: analog and digital.

ANALOG COMPUTERS

The term "analog," as applied to computers, pertains to representation by means of continuously variable physical quantities. For example, an analog computer can be a device that solves problems by setting up electrical circuits which represent the physical equivalents of certain phenomena and making measurements as these circuits are varied in accordance with changes in the phenomena. The analog computer is by no means restricted to electrical circuits as equivalents. The physical equivalents may be gear trains, gasses, fluids, and so on. A digital computer, on the other hand, is a device that solves problems by manipulating the numerical equivalents of phenomena in accordance with mathematical and logical processes. These numerical equivalents may be expressed as binary numbers, octal numbers, decimal equivalents, and so forth. In an electronic digital computer, the numerical equivalents are generally expressed as binary numbers; 1s and 0s. Values of voltage and current are used to represent the 1s and 0s of the binary numbers.

Analog computers, because of their nature, have some inherent limitations. The use of physical equivalents limits their versatility. They are limited to performing only the tasks for which they were designed or, in certain instances, closely related tasks. ADP systems using an analog computer as a central processor are also limited

They are designed to respond i
the numerical equivalent of th
Programming is merely a matt
and/or arranging these instruc
computers will respond in a pr
to a given situation. An ADP s
digital computer as its central
programmed to perform a wid
that may or may not be relat
more versatile than analog sys
tems are still limited as to the
they can perform by such fact

- The design of their cent
- The variety of input/out
- The programmer's capa
a numerical method for represe
the problem.

There are two basic types of d
special purpose and general pu

Special-Purpose Digital Comp

Special-purpose digital comp
to follow a specific set of inst
which are fixed at the time they
To change the operation of this
the actual construction of the
altered.

General-Purpose Digital Com

General-purpose digital c
instruction sequences which a
stored in memory prior to th
formance. This type of compu
be altered by inputting a
instructions. Since the opera
purpose digital computers can
relative ease, as compared to th
computers, they provide a f

registers (a series of electronic devices for porary storage of a binary word) counters (a s of electronic devices that progress through ecific binary sequence), and gates (AND or functions to set a flip-flop or generate a s condition signal). The computer manipu- binary numbers, (1s and 0s) representing erical values or conditions. Devices to retain e binary figures comprise the majority of the puter registers and each register has a nct purpose or function. Many operations ire that the binary word or data be trans- d from one register to another, and, possibly, al different words may be transferred simul- ously.

Gates are used to control the transfer of data ls from one register to another. These gates ist of diode and resistor networks. The gate it generates a signal to transfer the contents he register to another at a particular time if in conditions are met, such as if the instruc- being executed is an add, and if one of the bers being added is a negative number. If e conditions are met, a command signal is rated; if they are not met, the signal is not rated.

everal gates in the computer are active only ng specific instructions, such as divide, and, possibly, only during that instruction. On other hand, some gates generate signals that ommon to several instructions. In the design computer, each instruction that the com- r is to perform is very methodically analyzed, for each signal required, a gate is designated enerate the signal.

The size of the registers is relative to, and in determines, the general size of the computer. all registers in the computer have the same length. Some are determined by the accuracy ired, while others are determined by the uction word, number of addresses in the ory, and various other parameters.

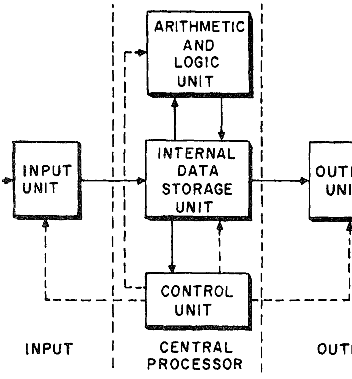


Figure 1-2.—Representative digital data processor, diagram.

dashed lines). The CP is composed of three units:

- Control Unit—This unit directs the all operation of the computer in accordance a prescribed plan.
- Arithmetic-Logic Unit—This unit forms the actual processing.
- Internal Data Storage Unit—This stores the data to be processed and the presc plan (program).

CONTROL UNIT

In a typical digital computer the co section includes the instruction register, the

The "P" register contains the address of the next sequential instruction to be executed. The contents of the "P" register are automatically advanced by one by the P + 1 adder.

General Register

This register stores the quantity used for address modification. In addition, it usually has the properties of automatic increment or decrement. Most computers have more than one general register.

SC Register

The SC register consists of one or two registers to accomplish the holding of a shift count. Its size is dependent on the maximum number of places that a word can be shifted.

CONTROL UNIT OPERATION.—An easy way to comprehend the operation of the control unit is to draw a comparison to a telephone exchange. The act of dialing a phone number energizes certain switches and control lines in a telephone exchange. In a similar manner, each program instruction, when executed, causes the control section to energize certain "switches" and "control lines." This enables the computer to perform the function or operation indicated by the instruction.

A computer program can be stored in the internal circuits of the computer or it may be read instruction-by-instruction from external media. The internally stored-program type of computer (generally referred to as a "stored-program" computer), is the most practical type to use when speed and fully automatic operation is desired.

In addition to the command which tells the computer what to do, the control unit also dictates how and when each specific operation is

that make up a "binary word,"
a specific operation that is to be p
location of the data to be operated
a part of the instruction and ene
which causes the specified o
subtract, compare, and so on) t
Subsequently, the control unit "r
instruction or jumps as directed t
instruction to execute.

Computer instructions are bro
four general categories. The in
transfer, arithmetic, logic, and c

Transfer commands transfer
location to another. One of the
usually an address in memory, a
either a register or an input/out

Arithmetic instructions comb
of data to form a single piece of
of the arithmetic operations. In
types, one of the pieces of data
specified by an address containe
tion and the other is already in a
the accumulator). The results ar
the accumulator.

Logic instructions make the d
much more than an expensive "ad
The use of logic instructions e
grammer to construct a progra
number of tasks. These instru
computer used for inventory
follow one set of procedures
items count is too large and anot
is too small. The choice of whi
dures to use is made by the co
the influence of the logic inst
instructions provide the comput
ity to make decisions based o
previously generated data.

Control instructions send
devices not under direct control
unit, such as input and output un
portion of the control instruction
a location in memory but is usuall

instruction may produce a result which tes that the next instruction is to be taken an address as specified in a portion of the instruction. For example, the logic instruc- may initiate certain operations in the com- to determine if the content of a given ter in the arithmetic section is negative. If nswer is "yes," the location of the next uction is specified in an address section of ogic instructions. If the answer is "no," the instruction would be taken from the next ential location in the memory.

very computer provides circuitry for a ty of logic instructions, thus providing the bility of selecting alternate instruction encies if certain desirable or undesirable itions exist. The ability to "branch" at key s is the special feature of the computer that es it able to perform such diverse tasks as le control, accounting, and tactical air ing.

THMETIC-LOGIC UNIT

he arithmetic-logic unit is the section hich arithmetic and logic operations are rmed on the input or stored data. The ations performed in this unit include adding, racting, multiplying, dividing, counting, ng, complementing, and comparing.

enerally, information delivered to the rol unit represents instructions, while infor- on routed to the arithmetic unit represents Frequently, it is necessary to modify an uction. This instruction may have been used e form in one step of the program but must tered for a subsequent step. In such cases, nstruction is delivered to the arithmetic unit e it is altered by addition-to or subtraction- another number in the accumulator. The tant modified instruction is again stored in nemory unit for use later in the program.

an accumulator ("A" register). During an metic process, the "D," "X," and "Q" reg temporarily hold or store the numbers used in the operation, called operands. accumulator stores the result of the opera The control unit instructs the arithmetic u perform the specified arithmetic operatio requested in the instruction). It then tra the necessary information into the "D," and "Q" registers from memory and contro storage of the results in the accumulator some specific location in memory.

The arithmetic unit also makes compar and produces "yes" or "no" or "go-no outputs as a result. The computer can be grammed so that a "yes" or "go" result c the computer to perform the next step i program, while a "no" or "no-go" instru may cause the computer to jump several grammed steps. A computer can also be grammed so that a "no" result at a certain in the program will cause the computer to and await instructions from a keyboard or input device.

INTERNAL DATA STORAGE UNIT

In some digital computers the internal storage unit, or memory section, is constr of small magnetic cores, each capable of r senting an "on" ("1") or "off" ("0") cond A system of these cores arranged in a matr store any computer word that is represen binary form.

All computers must contain facilities to computer words or instructions (which intelligible to the computer) until these in tions or words are needed in the performan the computer calculations. Before the st program type of computer can begin to op on its input data, it is first necessary to sto memory, a sequence of instructions ar figures, numbers, and any other data which computers use an auxiliary (wired) memory which permanently stores the "bootstrap program," thereby making manual loading unnecessary. These instructions may be stored in "chips" (referred to as ROMS).

The memory (or storage) section of a computer is essentially an electronically operated file cabinet. It is actually a large number (generally between 1 and 40,000) of storage locations; each referred to as a storage address or register. Every computer word that is read into the computer during the loading process is stored or filed in a specific storage address and is almost instantly accessible.

Storage Devices

The types of memory storage devices used most frequently in present-day computer technology are magnetic cores, semiconductor memories, thin film, magnetic drums, magnetic tapes, and magnetic disks.

MAGNETIC CORES.—One of the methods for storing internal data in a computer is realized by using magnetic cores. Cores are generally constructed by either of two methods. The first type of core, called a tape-wound core, is fabricated by wrapping a tape of magnetic material around a nonmagnetic toroidal form. A toroid is a term used to describe a doughnut-shaped solid object. The second type of core is called a ferrite core, and it is made by molding finely ground ferrite into a toroidal form. The ferrite used in this application is a ceramic iron oxide possessing magnetic properties. The ferrite particles are then heat-fused or "sintered" by the application of heat and pressure.

In magnetic core memories, each data bit is stored in the magnetic field of a small, ring-shaped magnetic core (figure 1-3). Magnetic cores generally have four wires running through them. Two wires are used for READ selection,

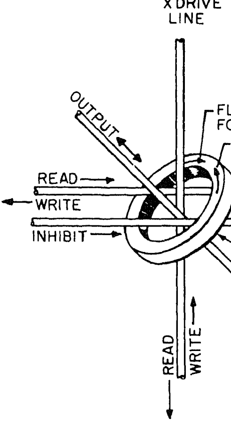


Figure 1-3.—Magnetic core sho
and sense l

These cores are arranged
and columns), to assign me
and quickly write data
read-out purposes. The
frequently for writing a
magnetic core arrays is kno
current technique.

In computer memory a
core is magnetized by a flu
a current flows in a wir
threaded through the core
large amount of this flux
removed. Flux lines can be
or counterclockwise aroun
upon the direction of the m
current in one direction est
tion in a core in a given di

mic. MOS means metal oxide semiconductor, LSI means large scale integration. We discuss this type of memory later in this ile part.

HIN FILM.—Thin film memory consists rmalloy, a ferromagnetic material, deposited er controlled conditions in a vacuum iber) on a supporting material (substrate) of glass. When all air has been removed from hamber, a shutter arrangement is opened apors from molten Permalloy pass through isk and are deposited on the supporting rial (substrate). The pattern thus formed is mined by the shape of the mask. The thick- of each spot (magnetized area) is controlled e amount of time the shutter is open.

magnetic field is applied parallel to the ce of the substrate during deposition. The spots become easier to magnetize in the tion parallel to that in which the magnetic was applied during the deposition process. direction is known as the preferred direction; ise, the axis of this magnetism is called the rred axis.

IAGNETIC DRUMS.—The magnetic drum ge device is a cylinder that rotates at a ant velocity. Information is written on or from the drum when its magnetic surface s under magnetic heads, which are similar e magnetic heads found on commercial tape ders.

lagnetic drums provide a relatively inexpen- nethod of storing large amounts of data. A etic drum (figure 1-4) is made from either low cylinder (thus the name "drum") or a cylinder. The cylinder may consist entirely magnetic alloy, or it may have such an alloy d upon its surface. Many drums are made praying on magnetite, an iron oxide. The ce is then coated with a thin coat of

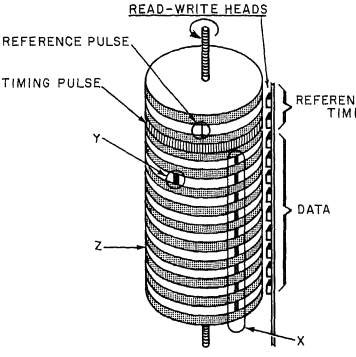


Figure 1-4.—Magnetic drum.

As the drum rotates, the tracks are tinuously passing under their respective Each track is subdivided into cells, ea which can store one binary bit. All the cell are positioned under the heads of a multi drum at the same time are called a slot. some drums, each head "reads" or "wr one bit of a word. Thus, when a word is w into or read from a slot, each track contain bit of that word. The number of heads depends on the size of the word that the puter is designed to handle.

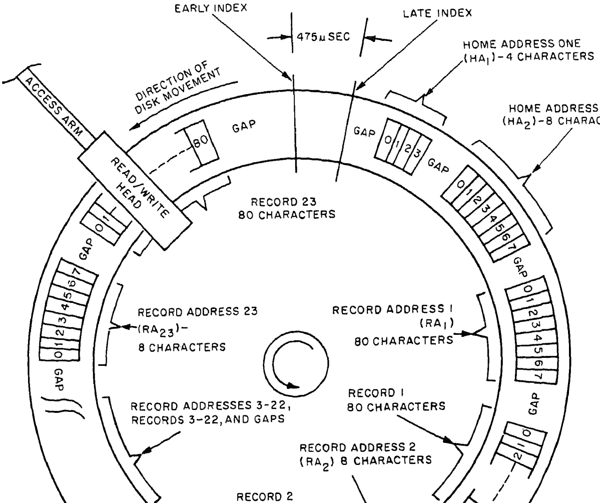
One of the tracks provides timing signa the drum rotation. The timing track deter the location of each set of storage cells ar the drum. Each timing signal denotes a u time of the drum rotation. For example, timing track is 80 inches long and timing si are recorded at 120 pulses per inch, ther

The retrieval of data from a rotating drum can be a rather involved process as can be realized by drawing a comparison to the core memory of a computer. When core memory is used, all the data is stored in the cores in a static condition. The data can be located at a given place at any instant and easily read from that location in serial or parallel form to represent the same data that was stored in that location.

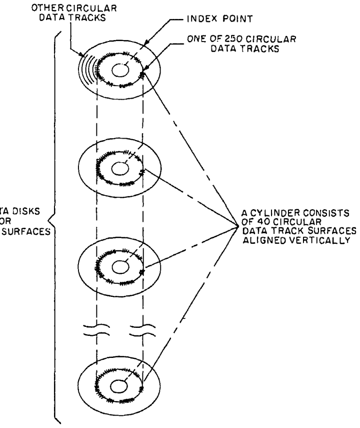
Transfer of the data from constantly rotating magnetic drums, on the other hand, is complicated. Timing pulses are not used to synchronize the drum speed (which may vary slightly from time to time). Thus, some method must be used to ensure that data read into the drum memory in a given bit position will be read from the memory with the same time
probability of an incompatible t
between the drum speed and sync
pulses makes it necessary to
means of compensating for va
speeds.

In practice, the drum con
point and a number of secto
format. The control point is a
that specifies a starting locatio
All data stored on the drum is r
indexing point or "reference p
figure 1-4).

MAGNETIC TAPES.—M
widely used as a storage me



se of its long access time. This is readily ted if one considers that needed information dely (and sometimes randomly) distributed the tape. Thus, the two main advantages e gained by using magnetic tapes are its storage capacity and low cost.


OTHER CIRCULAR DATA TRACKS
INDEX POINT
ONE OF 250 CIRCULAR DATA TRACKS
TA DISKS
OR
SURFACES
A CYLINDER CONSISTS OF 40 CIRCULAR DATA TRACK SURFACES ALIGNED VERTICALLY

164.44

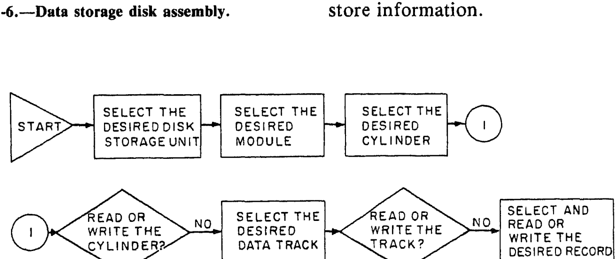
Figure 1-6.—Data storage disk assembly.

of mass volumes of production programs many applications, disks are superior to mag tape for rapid aquisition and storage of volumes of systems programs and data.

Magnetic disks resemble phonograph re that have been coated with iron oxide. The (or platters) are arranged in stacks in muc same way as a record stack in a "juke box. the disks are continuously revolving and sp apart so that a record head driven by an a mechanism can be positioned between the

Data is recorded at a certain address specified disk. When readout of a parti bit of data is desired, the recording he automatically positioned and the data is serially from the surface of the selected d

The basic unit of information on the d called a character. By design, each char contains a given number of bits (for fixed- applications). One or more of these charact a group form a record. A circular data (figure 1-5) consists of one or more rec associated record addressees, gaps, and track identification. A number of data t aligned on vertically arranged disks (figur form a cylinder of information. A magneti file system may contain one or more (modules). Each module contains a spe number of disks with their associated cyli and data tracks. The flowchart in figur illustrates the procedures necessary to retrie store information.


START
SELECT THE DESIRED DISK STORAGE UNIT
SELECT THE DESIRED MODULE
SELECT THE DESIRED CYLINDER
I
I
READ OR WRITE THE CYLINDER?
NO
SELECT THE DESIRED DATA TRACK
READ OR WRITE THE TRACK?
NO
SELECT AND READ OR WRITE THE DESIRED RECORD

INPUT/OUTPUT (I/O) DEVICES

I/O devices are similar in operation but perform opposite functions. It is through the use of these devices that the computer can communicate with devices external to the computer itself (peripheral devices).

Input Devices

Input data may be in any one of three forms:

- Manual inputs from a man-machine interface (MMI) such as a keyboard or console.

- Analog and/or digital inputs from instruments or sensors.

- Inputs from a source on or in which data has previously been stored in a form intelligible to the computer.

Computers can process hundreds of thousands of computer words per second. Thus, a study of the first method (manual input) reflects the inability of human-operated keyboards or keypunches to supply data at a speed that matches the speed of digital computers. A high average speed for keyboard operation is two or three characters per second, while, when coded to form computer words, would reduce the data input rate to the computer to less than a word per second. Since the computer can read several thousand times this amount of information per second, it is clear that manual inputs should be minimized to make more efficient use of computer time.

Instruments used as input sensors are capable of supplying several thousand samples regarding pressure, temperature, speed, and other measurements per second. This is equivalent to 10,000 to 20,000 bits or binary digits per second. Digital computers that use these devices must be equipped with analog-digital (A/D)

The most commonly used
category are magnetic tap
tape (perforated tape) read

Output Devices

Output information is a
three forms:

- Displayed informati
symbols presented on a
which are used by the
questions or make decision

- Control signals, t
which operates a control de
aileron, or actuator.

- Recordings, which i
in a machine language or
tapes or printed media.

Devices that store or r
tion include magnetic ta
punched paper tapes, catho
electric typewriters, and hi

One of the main featu
their ability to process la
quickly. In most cases, the
exceeds the ability of inp
information. One commo
input devices is that each in
ical operation; for exampl
tape drive or card feeder.
movement of some part of
take place fast enough
speeds with the computer
limit the speed of operati
computer. This is particul
where successive operation
the receipt of new data fro

Several methods of spe
operations have been devi

he comparative rates of data for these ms are:

- Card systems—2700 characters per second.
- Tape systems—350,000 characters per second.
- Disk systems—15,000,000 characters per second.

nother method of entering data into a puter, which we have not previously men- d, is to link two or more computers her and program them to communicate each other. This is perhaps the fastest od of entering or extracting data from a puter.

egardless of the type of input/output (I/O) e being used, the purpose of the I/O section provide the computer with access to these es.

he I/O section of a computer provides the ssary lines of communication and generates signals as are necessary for the computer stablish communications with and, where ssary, to control the operation of the I/O es. The I/O section, once it has been initiated ne control section, usually operates inde- ently of the control section except when it time-share memory with the control section.

INTEGRATED CIRCUIT (I/C) TECHNOLOGY

lodern digital computers are made with ICs provide the most economical and tical method of implementing the circuits ired to carry out the functions of a digital puter. In this section, we will discuss the s of ICs that make up modern digital

Small Scale Integration (SSI)

SSI circuits contain very little circ generally fewer than ten circuits no more co than a typical logic gate. Typical SSI ci include multiple logic gates, flip-flops, simple combinational logic circuits.

Medium Scale Integration (MSI)

MSI circuits are more complex and so ticated than SSI circuits. Most MSI ci contain twelve or more circuits equivale complexity to a typical logic gate. MSI ci are functional in nature in that they perfo specific logic operation with no further connection. Typical MSI circuits include cou shift registers, arithmetic-logic circuits, dec multiplexers, and other combinational sequential logic circuits. MSI circuits are l beneficial because they significantly cut d time. They also reduce the number of I design, minimize circuit wiring, and reduc and power consumption. Most digital equip can be implemented by simply combinin proper MSI circuits.

Large Scale Integration (LSI)

LSI circuits are large and complex generally contain circuitry equivalent to 1 more typical logic gates. LSI circuits are functional in nature. Typical LSI ICs in memories and microprocessors.

Very Large Scale Integration (VLSI)

VLSI circuits are large complex ci which contain the equivalent of 1000 or logic gates.

Most digital computers use a mix of MSI, and LSI circuits. Over the years, how the trend has been toward the greater use of LSI and VLSI circuits. Today, most com

These include bipolar and MOS devices. Bipolar ICs tend to dominate because of their flexibility and high speed. However, there is a trend toward the increased use of MOS circuitry. Since MOS technology has advanced over the past several years, improved circuits have become available making MOS circuitry more popular. Most microprocessors and semiconductor memories are MOS circuits. Therefore, entire digital computers can be economically implemented with MOS circuitry.

DIGITAL CIRCUIT CHARACTERISTICS

Many factors influence the choice of logic circuits used to implement a digital computer. The most important of these are speed, power dissipation, and the availability of MSI, LSI and VLSI circuits. Other factors include the cost, noise immunity, and interface capabilities.

The most important choice of a type of logic involves speed and power dissipation. Speed refers to the frequency of operation or propagation delay of the logic circuits. The higher the speed of operation, the greater the amount of data that can be processed in a given time. Therefore, computer designers try to achieve as much speed as possible in their designs.

Many high-speed circuits and techniques are available. Besides choosing circuits with low propagation delay times, circuit reduction techniques are used to minimize propagation delay through proper physical layout as well as logic simplification. However, speed is always obtained at the expense of increased power dissipation and cost. Invariably, the designer faces a speed-power tradeoff and attempts to optimize the design for maximum speed within realistic power consumption and cost guidelines.

Choosing ICs to use in implementing a digital computer involves not only choosing a specific logic family but also in choosing the correct mix of the various IC technologies

Their high speed, reasonable pow
low cost, and wide variety of MS
functions have made bipolar ICs
of most computer designers.
continue as improvements are r

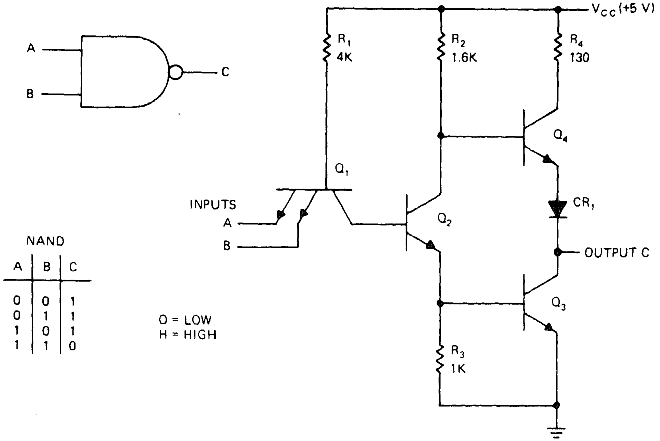
Of the many different ty
circuits available, transistor-tr
emitter-coupled logic, and integ
logic are most commonly used ir
computers. We will review each of
types.

Transistor-Transistor Logic (TT

Transistor-transistor logic
integrated circuits were introdu
1960s. TTL grew rapidly to be th
type of digital integrated circuit.
ments and variations have been
introduction, making it by far th
of the digital integrated circuit
TTL continues to be a popular
grated circuits, and it is by far
used in digital computers. It
balance between speed-power co
and availability of MSI, LSI and

A standard TTL logic gate is
1-8. This gate performs the
function. All other TTL funct
mented with this basic circuit
version of it. The most importar
of a logic gate are speed and pow
These are the characteristics tha
when logic circuits are evaluate
TTL logic gate shown in fig
average propagation delay time o
and a power dissipation of abo

A significant improvement
basic TTL circuit was made by
with Schottky transistors. A Sch
is essentially a bipolar transist
Schottky barrier or hot carrier
between its base and collector as

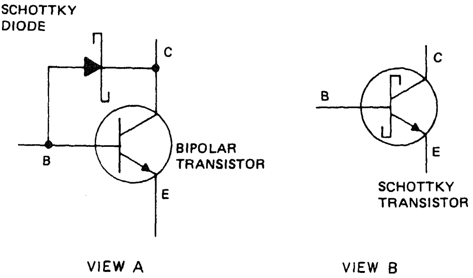


NAND

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

182

Figure 1-8.—A standard TTL logic gate.



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e 1-9.—(A) A bipolar transistor with a Schottky diode between emitter and base becomes a Schottky transistor;

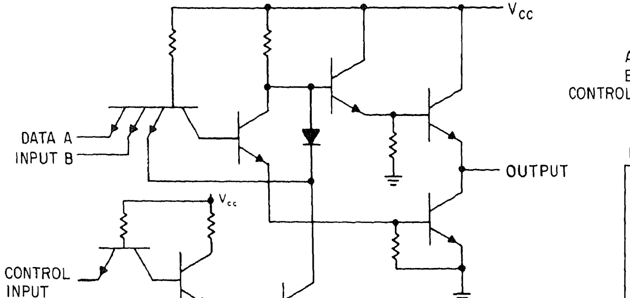
delay of about 3 nanoseconds, which is less than one-third that of the standard TTL gate. This increased speed is obtained with an increase in power dissipation to about 20 milliwatts and, of course, the higher cost of the Schottky technique.

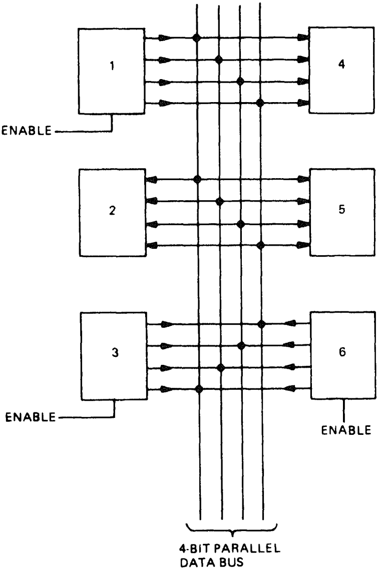
A low-power version of the Schottky TTL gate is also available. This device uses much larger circuit resistances, thereby considerably reducing the power consumption. At the same time, Schottky transistors are used to improve the switching speed. A typical low-power Schottky TTL gate has a propagation delay of about 10 nanoseconds, with a power dissipation of 2 milliwatts. A low-power Schottky gate has the same propagation delay as a standard TTL gate, but its power dissipation is one-fifth of the standard gate. These improved speed-power characteristics are obtained at only a slight increase in cost over the standard circuit. At present, the low-power Schottky TTL circuit is perhaps the optimum TTL circuit. This accounts for its high popularity with all digital designers. Low-power Schottky TTL is rapidly replacing standard TTL circuits

new designs.

Another TTL circui
puter applications is T
National Semiconductor
typical three-state TTL
table are shown in figu
a standard TTL NAND
of high impedance input
circuits are used in bus
designs.

A bus is a multiple co
which digital informati
other words, a bus is a
mission lines which are c
circuits. The outputs an
circuits are connected t
communication lines. Th
of digital design impro
and reduces wiring, asse
and testing costs. The in
various digital circuits us
a common bus. All co
these various circuits ta





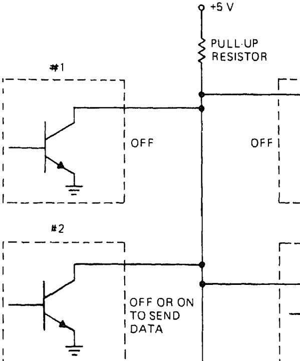
182.189.3X

Figure 1-11.—A 4-bit data bus digital system.

lines. This means that the bus is time-shared by the various circuits connected to it. Circuits applying data to the bus are multiplexed according to the desired data transfer. Figure 1-11 shows a simplified block diagram of a typical bus-organized system. Here, six digital circuits are connected to a 4-bit typical parallel data bus. Circuits 1, 3, and 6 apply data to the bus one at a time. The enable lines determine which circuit sends data to the bus. Circuits 2, 4, and 5 receive

one circuit may receive this info
inputs.

TTL integrated circuits cannot
drive a data bus. Directly connecting
of TTL circuits together will cau
operation of the circuitry and, in
cause damage to the circuits. The pri
for the inability to use TTL circuits
the active pull-up transistor (Q_4 in
This disadvantage has been overcom
a variety of open collector TTL circu
Open collector TTL circuits do not
active pull-up transistor. The colle
output inverter transistor is simply
to a pin on the integrated circuit and
pull-up resistor is used. Open co
circuit outputs can be connected dire
by using a simple pull-up resistor
figure 1-12. We say that the circuit
wired ORed. The gates not sending
bus line are controlled in such a wa
output is high and, therefore, the ou
transistor is off. In this way the ac



can control whether that line is high or low.

While open collector TTL circuits can be used in this way, many of the benefits of TTL circuits are lost by eliminating the active pull-up transistor. The high speed and high noise immunity associated with standard TTL circuits are lost when open collector circuits are used. To gain back these advantages and maintain the high speed and superior noise immunity of TTL circuits, the three-state TTL gate was developed.

Figure 1-10 shows a typical three-state TTL circuit. This circuit performs the positive NAND function. Its characteristics are similar to the TTL gate in figure 1-8. The main difference is the use of a control input which is used to effectively disconnect the circuit output from the IC pin. When the control input is binary 0 (low), the circuit functions like any other TTL circuit. It generates standard TTL logic 0 and 1 levels. However, when the control input is made binary 1 (high), both output transistors are cut off. With the circuit in this high impedance state, its output is effectively disconnected from the IC pin. With this arrangement, the outputs of any three-state TTL circuit can be connected to a common bus line. The control inputs of all circuits not sending data are made 1 and are disconnected from the bus line. Only the circuit that is to send data to the bus line is enabled.

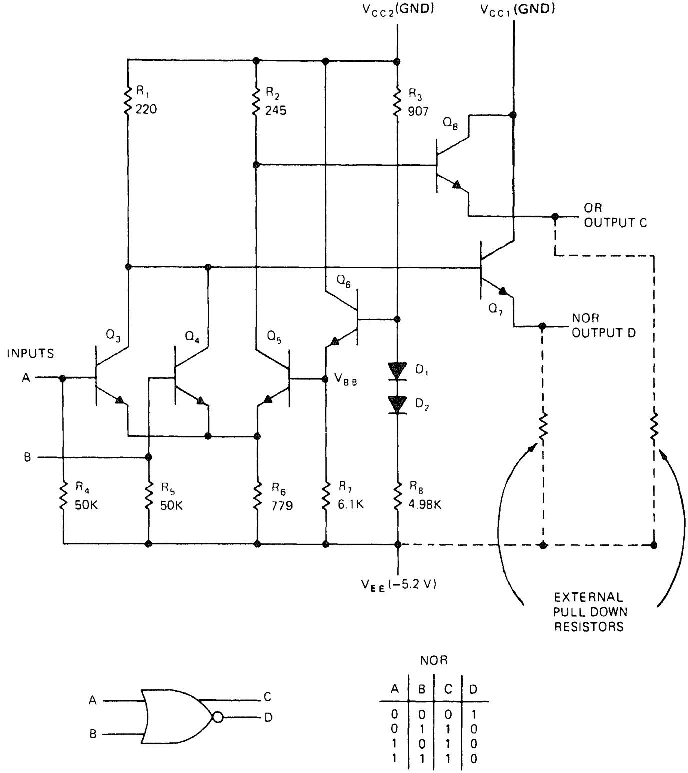
Emitter-Coupled Logic (ECL)

Emitter-coupled logic (ECL) is the fastest family of digital circuits available. Nonsaturating bipolar transistors and low resistor values are used in the circuit to achieve extremely high operating speeds. ECL circuits with a propagation delay as low as 1 nanosecond are available. A widely used type of ECL digital circuit is the 10,000 series manufactured by Motorola.

logic functions. Both SSI anc
available.

ECL circuits are used in
where speed is of primary i
speed is obtained at the expe
dissipation. Such high speed
complications. For example, th
between the various logic circ
as'short as possible. The prop
short piece of interconnecting
that of the gates themselves
propagation delays, interconn
be kept very short. This means
circuits must be very closely s
spacing creates integrated circ
packaging difficulties. High-d
difficult to construct and work
the close spacing also compou
dissipation problem. By co
circuits with high power diss
space, the heat buildup is s
special cooling techniques must
the excessive heat buildup. Des
and cost associated with the h
tion of ECL circuits, these p
sidered secondary where high s
necessity. A number of fast n
large scale digital computers u
phenomenally high data proc

When a computer desig
bipolar logic circuit with a pr
the 2 to 3 nanosecond range,
consider both ECL and Schott
and power dissipation of thes
practically the same. Becaus
dissipation performance of th
so close, the decision genera
factors. This choice more
to Schottky TTL because o
immunity, the greater ava
functions, and the ease of int



NOR

A	B	C	D
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

182.1

Figure 1-13.—A typical ECL logic gate.

Figure 1-14 shows a basic integrated injection logic circuit used in IIL networks. The basic circuit element is an inverter with a multiple collector output transistor Q_1 and a current source transistor Q_2. The current source transistor (called the injector) can also have multiple collectors to supply current to more than one common emitter inverter transistor. The emitter of the current source is connected to the external
supply voltage through a
the external resistor and t
the amount of injection
supply to the base of th
sufficient to cause the t
When the input to this ci
high state, current is supp
by the injector transistor
its collector outputs are
potential. When the inpu
near ground, the curren
diverted from the base o
cut off and its collector
These circuits are readil
interconnection and are
form a variety of logic g
circuits.

Figure 1-15 shows an
circuit symbol and truth
from Q_1 and Q_2 are wire
of Q_3. If both A and B
will be low. If either A or
will be cut off and C wi
positive NAND functio
multicollector transistor
current injector.

The primary advanta
conventional bipolar circ

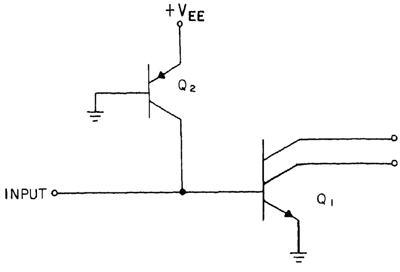


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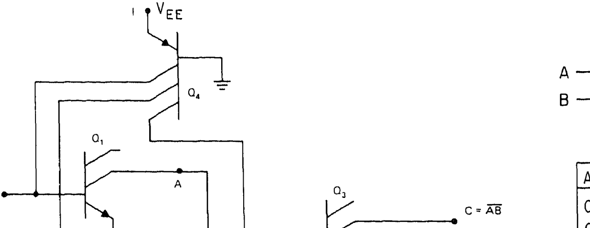
Figure 1-14.—A basic integrated injection logic circuit.



ity, low power dissipation, and relatively speed. Because of its simplicity, I^{2}L circuits be constructed in a fraction of the space ired by other bipolar circuits. About ten s as many I^{2}L logic circuits can be con-ted in the same space occupied by equivalent circuits. Over 2000 I^{2}L gates or similar its can be manufactured on a single silicon I^{2}L circuitry is even more economical hip area than the most advanced MOS its. One of the primary advantages of MOS rated circuits is their simplicity and high ity. About two times as many I^{2}L circuits be produced in the same space occupied by valent p-channel MOS circuits. N-channel S circuits have about the same density as I^{2}L its.

ow power dissipation is another advantage L circuits. The power dissipation is equivalent at of a typical n-channel MOS circuit. The er dissipation of a typical I^{2}L gate is in the nowatt to 70 microwatt range.

he typical propagation delays for an I^{2}L are in the 25 to 150 nanosecond region. This es the typical I^{2}L gate somewhat slower standard TTL logic circuits. However, y improvements are possible. For example, ttky diodes can be added to the basic I^{2}L it to improve its switching speed. Propaga-delays in the 10 to 15 nanosecond region are ible with Schottky I^{2}L circuits. I^{2}L circuits faster than most equivalent MOS circuits. use of the simplicity of the I^{2}L gate structure, essing and manufacturing techniques are r than for more conventional bipolar circuits. increases the circuit yield as well as cing the cost.

any sophisticated new electronic tech-es combine both analog and digital functions. n implementing such systems with integrated

Integrated injection logic is the newest of logic circuit available, and its full pot has not yet been realized. Improvements in and performance can be expected to fin circuits to be used in microprocessors and high performance LSI computer circuits.

MOS INTEGRATED CIRCUITS

Compared to bipolar integrated cir MOS integrated circuits are a relatively r development. As we mentioned earlier, means metal oxide semiconductor and desc a technique for making high-density, low-p integrated circuits. The basic circuit ele in MOS integrated circuits is a field transistor (FET), called a MOSFET. known as insulated gate field effect transi MOSFETs are simple three-element, vo operated devices. Like a bipolar transistor, state of conduction can be controlled. used in digital integrated circuits, the MOS are switched between their conducting nonconducting states.

The primary advantage of the MOS grated circuits over bipolar ICs is their density and low power consumption. Be MOSFETs are simpler than bipolar transi more of these devices can be constructed w a given area. Nearly twice as many MOS can be accommodated within the same spa equivalent bipolar devices. In addition, be of their high impedance nature, MOSFE cuits consume much less power than their bi equivalents. These two benefits have bro about the rapid development of MOS integ circuits and their increased widespread MOS integrated circuits are usually LSI de Few SSI or MSI MOS circuits are avai The most widespread application for circuitry is in semiconductor memories

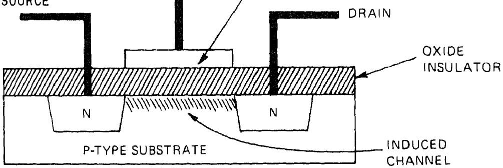


Figure 1-16.—An n-channel enhancement mode MOSFET.

be switched on and off. Figure 1-16 shows the construction of a typical n-channel enhancement mode MOSFET. The device consists of two n-type semiconductor areas fused into a p-type substrate. One of these n-type areas is known as the source and the other the drain. Between the source and the drain, a thin insulator is constructed between the substrate and a third metallic element known as the gate. The gate is the control element and the voltage applied to it determines the conduction between the source and the drain.

When the gate element is connected to the source or the voltage between the gate and the source is zero, the transistor does not conduct. That is, a complete current path between the source and the drain does not exist. However, when the gate is made positive with respect to the source, the electrons in the p-type substrate are attracted to the gate element. Because of the insulator between the gate and the substrate, gate current does not flow. However, the electrons will gather near the surface of the p-type material, thus forming a conductive channel between the source and the drain. This channel completes the electrical path between the source and the drain.

As you can see, an enhancement mode

The device we have just
n-channel enhancement mode
p-channel enhancement mode M
constructed by diffusing p-type
material into an n-type subst
construction is similar to tha
n-channel device. To cause the p
to conduct, the gate must be ma
respect to the source. This will
channel of holes to be formed be
and the drain. Both p-type ar
circuits are widely used in in
construction. Figure 1-17 show
used to represent n-channel MO
represents a generic presentation
MOSFET. The channel designa
be written adjacent to the syml
the type of device used. This meth
representation will be encour
figures in this module as wel
technical manuals. In view B t
toward the n-type material. The
on the line which represents
If the arrow points toward
indicates an n-channel with a p
If the arrow points away fr
it indicates a p-channel with
strate.

The earliest MOS integrat

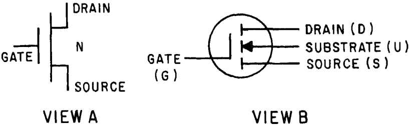


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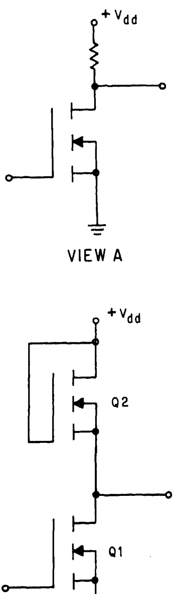
Figure 1-17.—The symbol used to represent an n-channel MOSFET.

type. N-channel MOSFETs can be made smaller and, therefore, more circuitry can be constructed in a given area. Since the n-channel device is smaller, it has less capacitance and can usually be made to switch faster than the p-channel device. N-channel circuits are preferred over p-channel equivalents because of their smaller size and higher operating speeds. In addition, they generally operate at lower positive supply voltages (typically +5 volts). This makes them compatible with TTL and I^2L integrated circuits. Despite these benefits, however, they are still more difficult to make than p-channel devices and, therefore, are usually more expensive.

MOS Circuits

The basic MOS logic circuit is the inverter shown in view A of figure 1-18. Here, a single n-channel MOSFET is connected in series with a drain resistor. When the gate voltage is zero volts or ground, the transistor does not conduct and the output voltage approaches the supply voltage V_{DD}. When a positive gate voltage is supplied to the gate, the MOSFET conducts. At this time, it acts as a very low resistance and its output voltage approaches ground. The

circuit. In fact, they occupy 20 or
the space of the typical MOS tran
resistors are not economical of ch
this reason, they have been mostl
from practical integrated circuits.
biased into conduction so that i
resistor is used in place of a stand
This technique is shown in view
1-18. Here, Q_1 is the standa
transistor. Q_2 is a similar MOS
gate is connected to the supply v
causes the device to conduct. Th
causes the MOSFET to act as a
resistance.



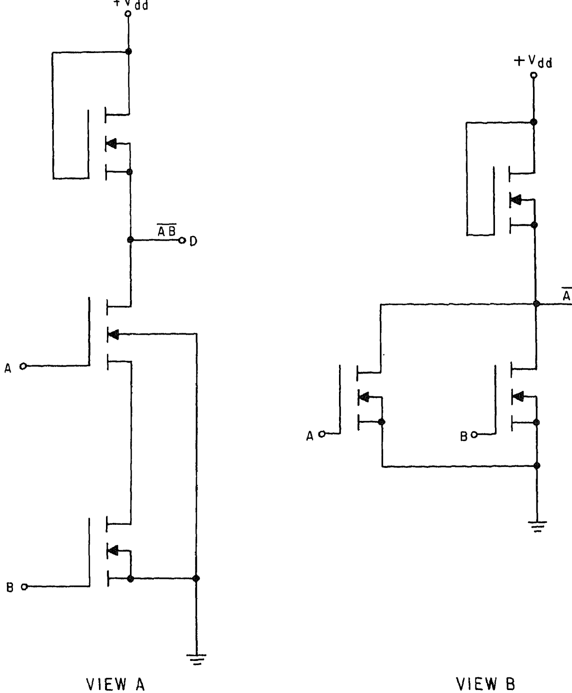
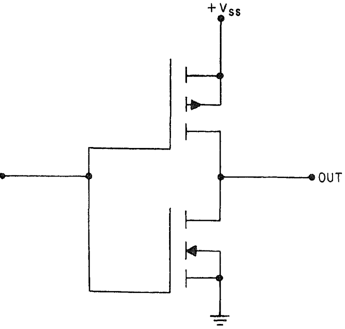


Figure 1-19.—Typical MOS logic gates. (A) NAND and (B) NOR.

MOSFETs are also readily connected to form a variety of logic gates. Figure 1-19 shows typical NAND and NOR logic gates constructed with MOSFETs. All MOS integrated circuits are some combination or variation of these basic

n-channel transistors. A ty
circuit is shown in figure 1-
zero volts or ground, t
MOSFET is properly bia
conducts. The lower n-cha



182.189.12X
Figure 1-20.—A CMOS inverter.

he primary benefit of MOS integrated
its is their extremely low power consump-
They consume less power than standard
r n-channel MOS circuits. The extremely
power consumption makes them especially
able for portable and remote applications.
ddition, the switching speed of a CMOS
it is typically faster than p-and n-channel
its.

he primary disadvantage of CMOS inte-
d circuits is the considerable amount of
area that must be used to construct
. They occupy about 10 times as much
e as the common n-channel MOS cir-
In fact, their chip complexity ap-
ches that of standard bipolar circuits.
reason for this complexity is the use of
p- and n-channel devices on the same
rate.

MOS LSI

The most commonly available MOS
grated circuits are LSI memories and r
processors. Practically all modern c
computers use MOS semiconductor mem
Both p- and n-channel memory element
widely used; however, the trend is towar
increased use of the faster and more
n-channel devices.

Another significant application of
devices is in the construction of microproce
Microprocessors are complete central proc
units or computers on a single silicon
The very high density of MOS circuitr
made such sophisticated complex devi
reality. Both p- and n-channel microproc
are available, although the trend is to
the use of the faster n-channel circuitry.
will learn more about MOS LSI memories i
section.

While high density and low power cons
tion are the primary advantages of
circuits over bipolar circuits, their disadva
is lower operating speed. Propagation d
of MOS circuits run typically 5 to 50
longer than those of equivalent bipolar d
(50 to 500 nanoseconds). MOS circuits c
be designed to achieve the high switching
that can be obtained with the bipolar cir
Over the years, MOS semiconductor techn
has greatly improved switching speed.
MOS devices still cannot achieve the
switching speeds as bipolar circuits, the
rapidly approaching those levels. Imp
n-channel and CMOS logic gates now
propagation delays considerably less tha
nanoseconds. Further improvements are exp
as new manufacturing methods and design
niques are discovered.

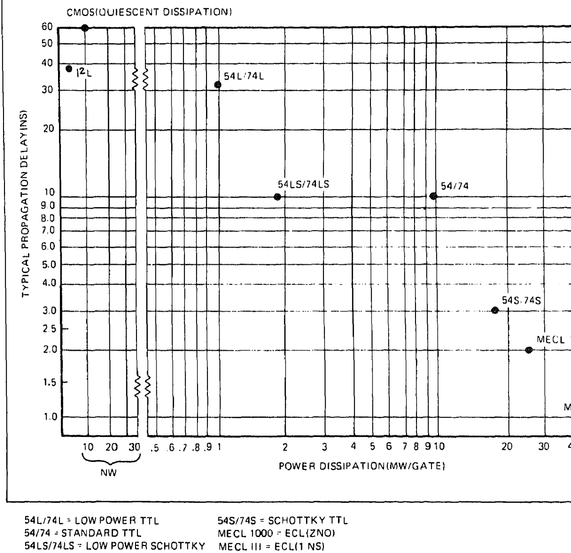


Figure 1-21.—Speed-power chart for standard logic gates.

LOGIC CIRCUIT COMPARISON

Figure 1-21 shows a speed-power chart for standard logic circuits. Power dissipation and propagation delay for all the logic circuits discussed in this section are plotted. This graphical means provides a convenient method of comparing the various logic families.

CENTRAL PROCESSOR

these two sections, they
be a single unit. Th
arithmetic-logic control
storage unit sections is u
central processing unit (C
then becomes a combin
input/output section. Mo
available today are sing
These devices are often
tion MPU or micropr

n will automatically carry out the func- specified. To do this, the control section es out a periodic fetch/execute cycle. In cycle, an instruction is read from memory, preted, and then executed. This fetch/ ite cycle is then carried out on the next uction in sequence. The fetch/execute is repeated until the program has been pleted.

ncluded in the control section of a computer a program counter (PC), an instruction ter (IR), an instruction decoder, and a g pulse generator. The PC contains the y address of the instruction to be fetched ogous to the "P" register). The starting ion of a program to be run is initially ed into the PC. The contents of the PC hen sent to the memory address register. nstruction decoder "looks" at the instruc- word and determines which instruction be executed. Like any decoder, only of its many outputs is enabled at a time. timing pulse generator, after receiving nput from the instruction decoder, generates quence of control pulses that are sent he memory, arithmetic-logic, and input/ ut sections to carry out the functions fied.

he timing pulse generator contains a ty of logic circuits, including a clock numerous logic gates that determine the and number of pulses needed. Besides nputs from the instruction decoder, the g pulse generator also receives inputs other sections of the computer. These outputs of other decision-making logic its which help to determine the operation e control section. For example, the control on may monitor the most significant bit he accumulator to determine the sign of umber stored there. Or, it may monitor a

Primarily, these signals have three pr functions:

- Gate or steer word transfers be registers.
- Determine the function of arithr logic circuits.
- Carry out various housekeeping operations, such as clearing a regis incrementing a counter.

All digital computer operations are r elementary. They consist of the movin data from one place to another anc processing of that data initiating logic tions that permit the first two to take It is the purpose of the control sectio see that these various fundamental o tions are carried out in the prope quence.

There are many different ways of i menting the control section of the c computer. For example, the control se could be implemented with SSI and MS cuits from the standard TTL or ECL families. Or, the control section ma implemented with MOS LSI circuits. control section of a microprocessor is i mented in this way. More important the method of implementation is the tecture or basic organizational concept c control section. The control section ca made with random logic circuits where va counters and combinational logic circuit combined to form the desired control p While older computers used the random method, most modern digital computer microprogramming with a read-only me (ROM) or programmable logic array. Ir section, we will discuss the various typ

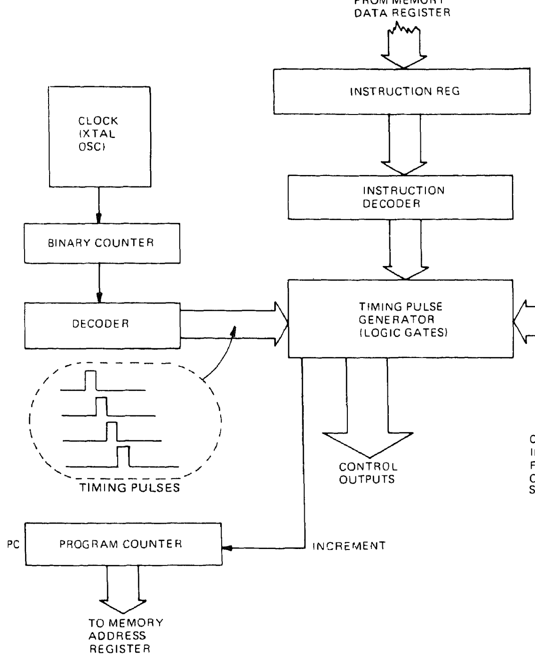


Figure 1-22.—Block diagram of a control section implemented with rand

Figure 1-22 shows a simplified block diagram of a control section implemented with random logic.

The instruction register (IR) receives its input from the memory during the instruction fetch cycle. The instruction decoder monitors the output of the IR and generates the output signals that

arithmetic-logic unit,
zero or negative, or
signal from an input/o
trol signals generated
distributed to other sec
One of the output co

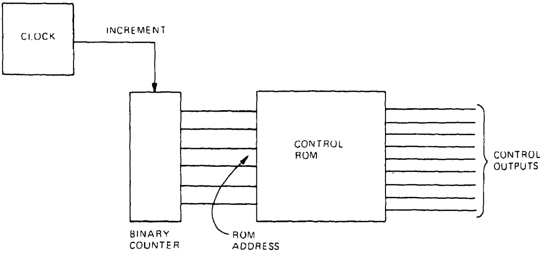
ype of implementation is inflexible in that nnot be easily changed.

he random logic method of implementation e most widely used method. However, oved techniques are now available and are kly becoming the more predominant method ontrol. These include microprogrammed rol systems and programmable logic arrays As). We will discuss PLAs later in this module

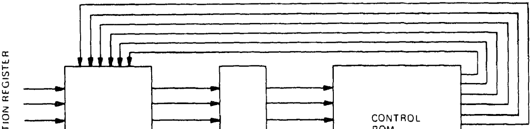
MICROPROGRAM CONTROL.—Microramming is a method used to build the conlogic of a digital computer. The heart of a oprogram control unit is a Read-Only ory (ROM). This ROM, when combined other logic elements, forms a flexible sequenlogic circuit that generates the desired rol pulses to implement the computer instrucset. This circuit is called a microprogrammed rol unit or a microcontroller.

A microprogram control unit is referred to as a computer within a comp The ROM in the microprogram control is analogous to the main computer mer The words stored in the control unit contain the information that generates control pulses. These words, usually ref to as microinstructions, are analogous t regular computer instructions stored in memory. The microprogram controller effec fetches and executes the microinstruction at a time to generate the control pulse does this in much the same way as the troller itself; sequentially reading and exec the instructions stored in the computer me to carry out the program. The microprogran control section is programmed by st the desired microinstructions in the co ROM.

A simple microprogrammed control u shown in view A of figure 1-23. It consists



VIEW A



ROM and a binary counter incremented by the system's clock. Stored in the ROM, at sequential locations, are binary words or bit patterns that when sequentially read from the ROM generate the desired control signals which include data transfers and the initiation of arithmetic operations and other functions.

Each ROM output bit is assigned a specific control function. The correct pattern of binary 1s and 0s is stored in the ROM. As the clock pulses occur, the binary counter sequentially accesses the ROM locations, reading the bit patterns out of memory.

A more sophisticated microcontroller is shown in view B of figure 1-23. Again, the ROM is the predominant component. Its operation is similar to the simplified circuit discussed previously in that the binary states appearing at the ROM output generate the desired logic operations. The output word and sequence are determined by the binary address supplied to the ROM by the ROM address register. The ROM address register receives its input from two sources. A mulitplexer selects the input source. First, an address can come from the instruction register (IR). This binary code (the op code), when loaded into the address register, causes a particular word sequence stored in the ROM to be used. The op code from the IR effectively defines the starting address for a microprogram in the ROM that will generate the control pulses necessary to carry out that instruction.

Note that the ROM address register can also receive an address from the output of the ROM itself. This means that a portion of each microinstruction contains an address that defines the location of the next microinstruction in sequence. Essentially, the starting address is received from the IR while the address sequence to be used is obtained from the microinstructions themselves. By obtaining the ROM address from the microinstruction itself, branch and sequential operations are easily obtained. For each instruction defined by the computer instruction set, a sequence of microinstructions stored in the ROM

functions, almost any desi
be implemented. For this r
set of microprogrammed c
very large and versatile. Wi
controller, more instructio
at a lower cost than with r
The only limiting factor is
Semiconductor ROMs are
usually permit the contro
mented at a lower cost th
logic controllers.

By making the ROM in
control unit replaceable, n
tion sets can be used with th
removing one ROM and p
nature of the digital com
completely. A digital comp
for a particular functio
proper instruction set anc
a control ROM. This per
emulate, or behave exactly
written in the machine lan
can be executed on ano
microinstructions stored in
required operations. Emu
widely used to minimize t
from one computer to ano
puter purpose changes
computer system is upgr
users have a significant i
grams (software) whose v
of the hardware (equipme
to use all the existing p
computer, emulation is son
the software investment
improved performance wi

In some sophisticated
ROM in the control unit
read/write memory. The
a writable control store.
microinstructions can be w
so that its contents can b
the characteristics of the

The primary disadvantage of a microprogrammed control unit is its lack of speed. It takes a finite period of time to access the microinstructions in the control ROM and read out a microinstruction sequence. Even with higher speed ROMs the instruction execution speed is limited. Higher speed operation can often be obtained with random-logic controllers. Despite this disadvantage, however, the speeds obtainable with microprogrammed controllers are more than adequate for most digital computers.

PROGRAMMABLE LOGIC ARRAYS (PLAs).—Another method of implementing the control logic in a digital computer is with a PLA. A PLA is a large-scale integrated circuit that can be used to replace random logic or ROM in the control section. The PLA offers significant improvements in performance over both random logic and ROM designs. As a result, PLA implementation of the control section of the digital computer is rapidly becoming the most predominant method.

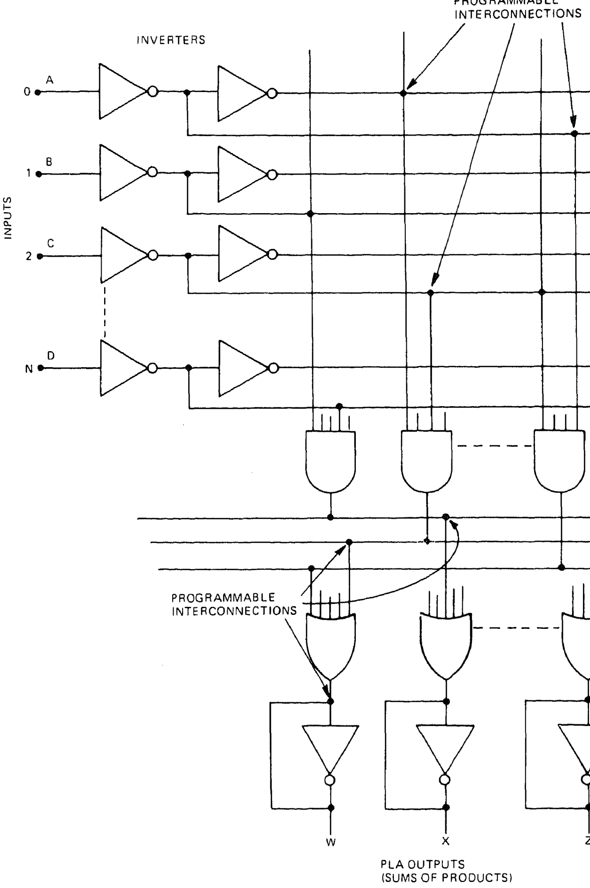
A PLA is a bipolar or MOS logic network that can be programmed during manufacturing to produce a logic circuit capable of replacing random combinational circuits or ROMs. The PLA is essentially a combinational logic circuit with multiple inputs and multiple outputs. Through programming, it can be made to convert any binary input code into any desired output code.

Basically, a PLA consists of a large number of AND and OR gates that can be interconnected to generate the sums of partial products. The AND gates monitor the inputs and generate minterms that are then combined in the OR gates to produce the desired outputs. In dealing with Boolean algebra, minterm is defined as the sums of the products of an expression. The inputs to the AND gates and the OR gates can be selected by the designer. When the PLA is manufactured, the wired interconnections are

by programming the connections
gates whose outputs are then com
gates to form the final outputs. A
tion of the sums of the vario
generated can be produced by p
necting the AND gate outputs to
inputs. Finally, note that the PLA
be programmed to produce the
complement output by simply prog
presence or absence of an inverter a
point.

With this flexibility, a PLA c
used to implement the control fu
digital computer. The inputs to the
monitor the op code of the instruc
and logic inputs from other sec
computer. The outputs generated
would control the various dat
arithmetic operations, and other log
The PLA offers a convenient, f
compact way of implementing
control logic. Because the PLA is an
its benefits are realized only in
where large numbers of inputs
are required. This is also true o
microcontroller. Where only a
inputs and outputs are needed, the
tion is more efficient with SSI o
circuits.

We have described the PLA
grammable LSI circuit that can be
generate a large number of sum
products. The PLA is a combin
circuit with multiple inputs and m
puts. However, there is another wa
the PLA. The PLA is a special ty
where the data addressing is prog
well as the data itself. As you learne
a ROM consists of an address d
decodes all possible states of the mu
input. The address lines or decode
then connected during the program
the various bit outputs, dependin
desired output word. As you can see


PROGRAMMABLE
INTERCONNECTIONS
INVERTERS
INPUTS
0
A
1
B
2
C
N
D
PROGRAMMABLE
INTERCONNECTIONS
W
X
Z
PLA OUTPUTS
(SUMS OF PRODUCTS)

memory locations are needed. In many ROM applications, large numbers of memory locations go unused. The circuitry and chip space are wasted, thereby making the ROM a less efficient device. The programmable address feature of the PLA overcomes this disadvantage.

The outputs of the AND gates for decoders in the PLA are then connected to the output OR gates to program the data at each location. In this respect, the PLA is similar to the ROM. When looking at a PLA in this way, it is considered to be a ROM with programmable addressing as well as data.

Since the PLA is effectively a ROM with programmable address and data, the PLA can be used to replace the ROM in microprogrammed controllers. In this application, the PLA is used in the same way. The PLA receives its input address data from the instruction register of the computer. Other inputs from other sections of the computer can also be accommodated. The PLA outputs then generate the control signals for the computer. Other PLA outputs can also be used to determine the input address sequence as done in ROM microprogrammed controllers.

The PLA is the most effective, efficient, and economic method of implementing control logic in a digital computer and is therefore becoming the predominant method for implementing such control. Its primary disadvantage is the need for programming during the manufacturing stage. For this reason, PLAs cannot be justified for low-volume designs. However, field programmable PLAs are becoming available which apply the field programming techniques used in programmable read-only memories (PROMs) to PLAs, thus making them more practical.

Arithmetic-Logic Section

The arithmetic-logic section of a digital computer is that group of logic circuits that

computer. Data to be processed is
the accumulator prior to the exec
instruction. In larger and more s
computers, multiple registers are
arithmetic-logic section. Data to b
is loaded into these registers. Da
between registers can be programm
tion, a wide variety of arithmeti
operations can take place betwee
stored in the various registers.

The unit that actually performs
arithmetic-logic operations is the
logic unit or ALU. The ALU is a co
logic circuit that processes data
ways. In simple digital computers
performs only a few basic function
common function is addition. Howe
modern digital computers, the AL
many other arithmetic and logic
These include addition, subtractio
mentation, comparison, shifting,
Boolean functions, such as AND,

The ALU receives input data
sources. In a simple digital comput
sources are the accumulator and
data register. In computers with multi
the ALU inputs come from these re
output of the ALU is applied to
receive the result of the arithmetic-
tion. In a basic digital computer
deposits its results back into the a
In multiple register arithmetic-log
the destination of the ALU output is
by the type of register instruction

TYPICAL ALU.—There are ma
ways of implementing the ALU wi
SSI and MSI combinational circuit
understand this, we will analyze the
ALU. This is a transistor-transistor l
scale integration (TTL MSI) combina
that performs practically all arithme
operations required. The 74181 per

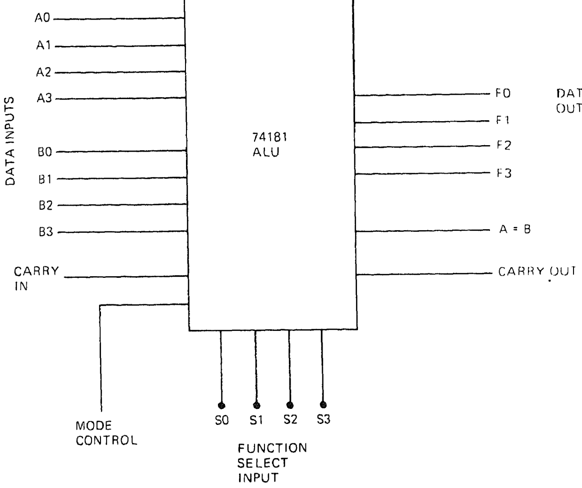
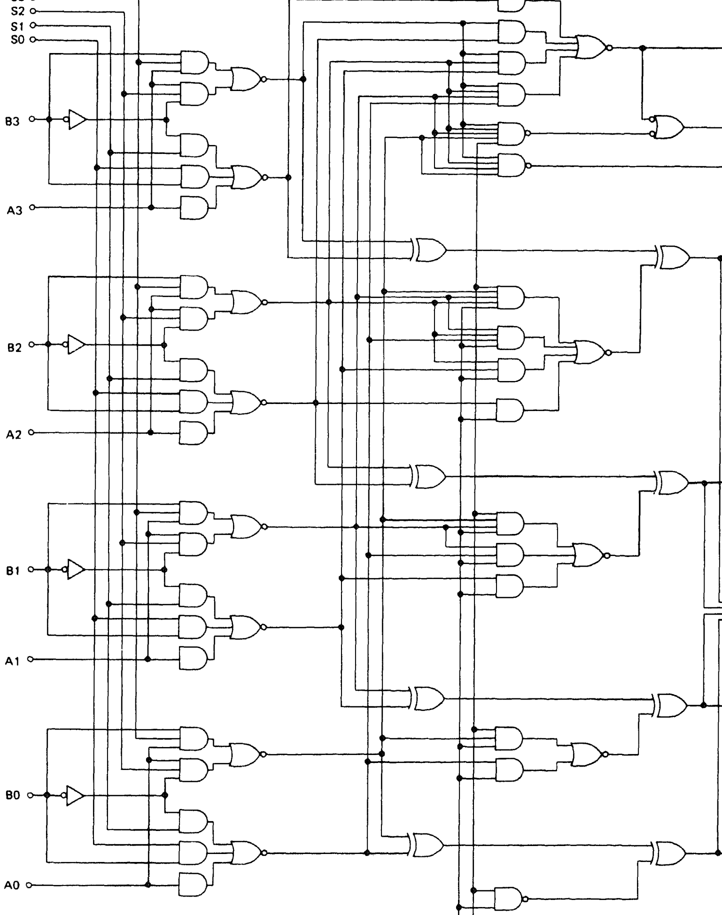


Figure 1-25.—General block diagram of 74181 ALU.

Figure 1-25 shows a general block diagram of the 74181 ALU. The bits of input word *A* are labeled A0 through A3. The bits of input word *B* are labeled B0 through B3. The output bits are labeled F0 through F3. The 4-bit function select code input bits are labeled S0 through S3. Other input and output lines include carry input and carry output lines which are used in cascading these units. The A = B output line is the comparator output which is used in cascading these units. The A = B output line is the comparator output which goes high when the *A* and *B* input words are equal. The mode-control line determines whether arithmetic

Table 1-2.—Logic table fo

SELECTION				ACTIVE-HIG
				M = H
				LOGIC
S_3	S_2	S_1	S_0	FUNCTIONS	$C_n = 0$ $\overline{C_n} = 1 = H$
L	L	L	L	F = A	F = A
L	L	L	H	$F = \overline{A + B}$	F = A + B
L	L	H	L	$F = \bar{A}B$	$F = A + \bar{B}$
L	L	H	H	F = 0	F = MINUS 1 (2's COM
L	H	L	L	$F = \overline{AB}$	$F = A$ PLUS $A\bar{B}$
L	H	L	H	$F = \bar{B}$	$F = (A + B)$ PLUS $A\bar{B}$
L	H	H	L	$F = A \odot B$	F = A MINUS B MINU
L	H	H	H	$F = A\bar{B}$	$F = A\bar{B}$ MINUS 1
H	L	L	L	$F = \bar{A} + B$	F = A PLUS AB
H	L	L	H	$F = \overline{A \odot B}$	F = A PLUS B
H	L	H	L	F = B	$F = (A + \bar{B})$ PLUS AB


S2
S1
S0
B3
A3
B2
A2
B1
A1
B0
A0

the 4-bit input selection function code to the state indicated in the left-hand column (refer to the logic functions column in table 1-2). As you can see, all the basic Boolean functions are represented. These include AND, OR, NAND, NOR, X-OR, and X-NOR. For example, when the function input code is HLHH (one represents a high and zero represents a low 1011), the AND function (F = AB) is performed on the input data. Each pair of bits is individually ANDed as indicated below:

A3A2A1A0 = 0101

B3B2B1B0 = 0011

F3F2F1F0 = 0001

Note also that the outputs can be set to all 0s or all 1s with function codes LLHH (0011) or HHLL (1100), respectively. In addition, A or B inputs can be connected directly to the F outputs (F = A, F = B). The complement of the A inputs or B inputs can also be connected to the output ($F = \overline{A}$, $F = \overline{B}$). Numerous other Boolean functions can also be performed as you can see by the table.

When the mode-control input line is low, arithmetic operations are performed. The specific arithmetic operation performed depends on the state of the carry input line. Both 1s and 2s complement addition and subtraction can be carried out with this circuit. Increment and decrement functions can also be performed. A special case is the F = A PLUS A operation designated by the input code HHLL (1100) when the carry input is high. This effectively causes a shift-left operation where each bit is shifted to the next most significant bit position. Binary 0s are shifted into the vacated least significant bit position. While the 74181 can implement such shift functions, shifting and rotating of data are

subroutine that perform
a shift and add algori
programmed in a similar
tic functions, such as squa
functions, can also be
addition, subtraction, sh
tions. The same is true fo
(BCD) arithmetic operat

Some larger digital c
wired arithmetic multiply
One method of implem
in a 74181-based ALU
function and register
microprogrammed contr
stored in the ROM or P
specific add and shift or
carry out the multiply
The four-function selec
would be driven directly
in the instruction regis
outputs of a ROM or
grammed controller.

Memory Section

Semiconductor mem
programs and data in a
puters. These memories a
electronic circuits and a
store many multibit bina
ductor memories are MO
some bipolar circuits
applications.

MAGNETIC CORE
different types of elect
circuits can be used as
computer memory. Hov
are practical and wi
memory element in some
magnetic core. As we ha

magnetized in the opposite direction. The cores are magnetized by causing current to flow in a wire through the core in one direction or the other. Data is read out of a core memory by changing the states of the cores and monitoring the output that occurs on a sense line passing through the cores.

While some computer systems still use core memories, newer digital computers use semiconductor memories. Semiconductor memories are less expensive, faster, more reliable, denser, and consume far less power than magnetic core memories. Semiconductor memories provide these advantages over any other type of memory circuit.

VOLATILITY.—The only real advantage of core memory systems over semiconductor memory is their nonvolatility. Semiconductor memories use binary circuits which can assume one of two states. Such memories require power to be applied at all times. If power is removed, all data storage is lost. Such memories are said to be volatile. Core memories are not volatile (also called nonvolatile). Since the cores can be magnetized, they will retain the data when power is lost.

The volatility of semiconductor memories was a distinct disadvantage in their initial stages of development. However, the volatility problem has been overcome in several ways. In many computer systems the memory power is never removed. If it should accidentally be removed by power-line failure, special battery or generator backup power supplies take over to ensure against the loss of data. Many semicondutor memories have such low power consumption that they can be operated continuously with small batteries for an extremely long time. The wide use of ROMs in which programs and data are permanently stored has also offset the disadvantages of volatility.

later. A ROM is one in which pro
data are permanently stored. In ot
data is written into the memory
manufacture. Thereafter, it cannot b
In this type of memory, data
written into the memory under progra
The data can only be read out. This
memory is widely used to store
and data in small computer syst
the computer is dedicated to a speci
tion.

Both read/write memories and
random-access memories. A RAM
of storage medium in which the c
any memory location can be a
random at essentially the same ti
other location. In other words, t
of time it takes to store or reac
in a RAM is essentially fixed for a
in the memory. Although both reac
ROMs are usually of the random-a
only read/write memories are genera
to as RAMs.

RAMs are far more desirable than
access memories in which the d
can be accessed only at certain
shift register is an example of
sequential-access memory. Seque
memories usually store binary dat
form. This means that the binary
stored or read out a bit at a
words are stored end to end and r
When data is accessed, it may
the correct position for readout. It
for the desired data word to cir
the correct position to enable the
The data access time in a serial mem
and its value depends upon the re
tion of the data in the storage
the time of the read request. Seque
memories are still used in some a
but most semiconductor memori

with which the program is executed.

MEMORY ORGANIZATION.—All semiconductor memories, both RAMs and ROMs, are organized as many storage locations for fixed-length binary words. The binary words are stored and read out in parallel.

The basic element of a semiconductor memory is the storage cell. Each storage cell is an electronic circuit that stores one bit of data. These cells are organized into multibit storage locations that can store a single binary word. For example, an 8-cell location is capable of storing a single 8-bit binary word. All of the cells in a given memory location are accessed simultaneously so that the data bits are written into them or read from them at the same time.

Each memory location is given a unique address. When the memory recognizes this address, data can be written into or read from that word location. The address is also a multibit binary number. A decoder in the memory "looks" at the address word and then enables the memory location specified by the address. Only one word in the memory is addressed or accessed at a time.

Figure 1-27 shows a typical block diagram of a semiconductor memory organization. It consists of a large group of storage elements organized into locations—each capable of storing a binary word. A multibit binary word known as the address is applied to the address decoder circuit in the memory. The decoder recognizes the unique address and specifies the unique memory location. Data can then be written into or read from that memory location.

Since the address word is a binary number, the total number of storage locations in a

8-bit address word and
locations for 8-bit word
a total of 8 × 256 = 2

One common semi
store 1024 one-bit word
can define 2^{10} = 1024
capable of storing a si
are then grouped togeth
form larger multibit w

The size of a se
defined by the total
the memory. This is u
of its number of me
number of bits in ea
the memory in figur
but is organized as
other words, it is a 256
The 1024-bit memory j
as a 1024 × 1 unit.

Another shorthand
memories is the use of
memories larger than
example, the 1024 ×
earlier is usually called
The exact power of 2
is rounded off to its
interval. For example,
16,384 word memories
8*k*, and 16*k* units, res

READ/WRITE
discussed earlier, re
memories are more fr
access memories or R
digital computers whe
read data from mem
memory under progr
digital computer give
grammer full flexibili
of program to be run
It is the RAM that

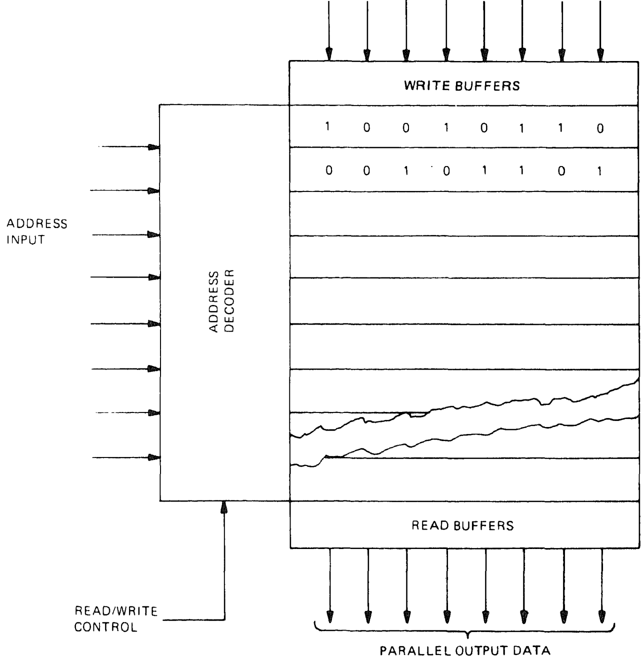
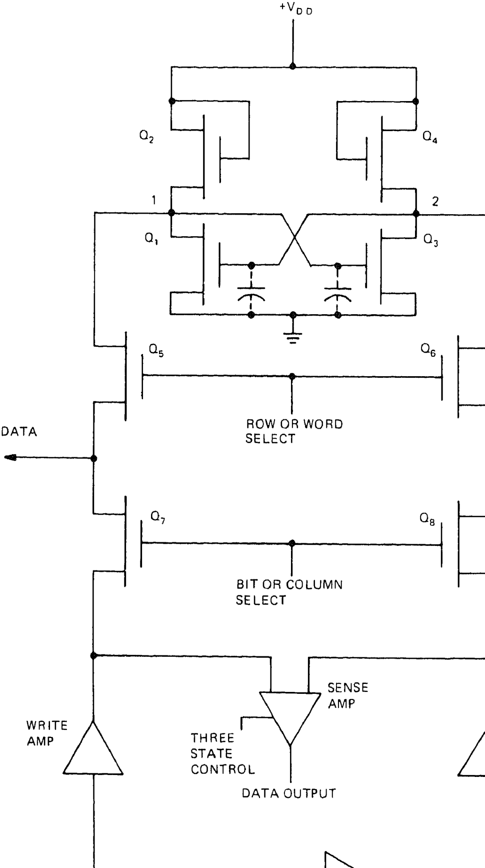


Figure 1-27.—Typical semiconductor memory organization.

memory cell is the electronic circuit that stores a single bit of data. Both static and dynamic cells store data on the gate capacitance of a MOSFET. The small gate capacitance between the source and gate of a MOSFET is on the order of several picofarads or less. When this

a standard two-state flip-flop is store one bit of data. In the dynami gate capacitance is the sole stora It operates a MOSFET whose outp conducting condition is sensed to whether a binary 1 or a binary


+V_DD
Q_2
Q_4
1
2
Q_1
Q_3
Q_5
Q_6
ROW OR WORD SELECT
DATA
Q_7
Q_8
BIT OR COLUMN SELECT
SENSE AMP
WRITE AMP
THREE STATE CONTROL
DATA OUTPUT

tatic Memories.—A typical static RAM ory cell is shown in figure 1-28. The ools used to represent the MOSFETs in case are generic in nature. It must be ted out at this time that although the FETs represented are n-channel, an equiv- circuit could be constructed with p-channel es. Although the theory of operation d be the same, the power supply volt- would differ if p-channel devices were .

he cell in figure 1-28 consists of two -coupled MOSFET inverter stages. One ter stage is made up of Q_1 and Q_2 the other inverter stage is Q_3 AND Transistors Q_1 and Q_3 are the inverters transistors Q_2 and Q_4 are the load tors.

he cross-coupled inverter stages form a dard direct-coupled latch or flip-flop. In type of circuit, when Q_1 is conducting, s cut off. When Q_3 is conducting, Q_1 t off. The conduction of the MOSFETs termined by the charge on the gate capaci- es of Q_1 and Q_3. If the gate capacitance $_3$ is charged, Q_3 conducts and the voltage s drain (point 2) approaches ground. The ge at point 2 then is below the gate hold voltage of Q_1. The charge on the capacitance of Q_1 assumes this voltage . Therefore, Q_1 is cut off and its output ge at point 1 rises toward the supply voltage . The charge on the gate capacitance $_3$ is maintained by Q_4, which is conducting. flip-flop remains in this state until external ges are applied to the circuit to change This flip-flop state can represent either ary 1 or a binary 0, depending upon the ce of the designer. The opposite binary state hieved by causing Q_1 to conduct and Q_3 to ff.

enabled. The sense amplifier generate proper logic output voltage levels. The o is usually buffered by a three-state devi that its output can assume either of the binary voltage levels or an open or impedance state. In the open or high impe condition, the buffer is effectively di nected from the data output pin. This arr ment is similar to that used in three TTL circuits. This permits the output static RAMs to be connected together bus-organized manner. The state of the t state buffer is determined by a chip-en signal. If the chip-enable input sign a logic 1, the output circuit is enabled, the state of the memory cell is fe the output. When the chip enable is 0, the output buffer is put into the impedance state and the cell output doe appear at the data output pin. The t state enable line is often called the chip line.

To store data into the cell, the de logic is applied to the data input. The input drives an inverter which gene complementary logic signals that are ap to write amplifiers. The desired storage is selected by enabling the row-select causing Q_5 and Q_6 to conduct. The co select line is enabled, causing Q_7 an to conduct, thereby applying the compleme signals from the write amplifiers to the and $\overline{\text{data}}$ lines. The complementary logic si on the data and $\overline{\text{data}}$ lines then forc and Q_3 to assume the desired states. example, if the data line is high an $\overline{\text{data}}$ line is low, the gate capacitance o will be charged and Q_3 will conduct. zero level on the $\overline{\text{data}}$ line effectively charges capacitance of Q_1, causing it to off.

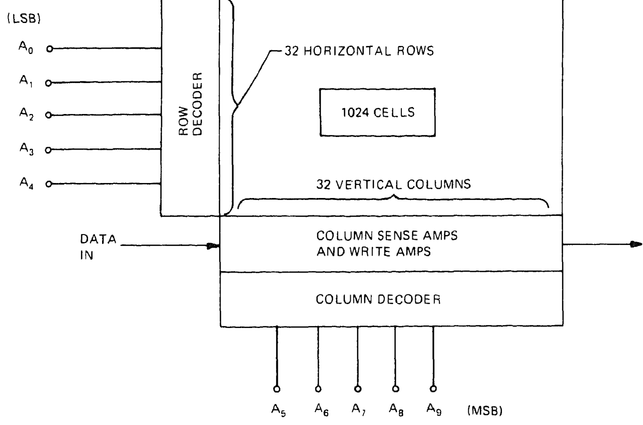


Figure 1-29.—Organization of a 1k × 1 static RAM.

figure 1-29. The five least significant bits of the 10-bit address word ($A_0 - A_4$) are used to drive the row decoder. The five address input bits are fully decoded into 32 enabling output lines. These lines, called the row-select lines, are each connected to the row-or word-select lines on 32 of the static storage cells. Only one of the 32 rows is enabled at a time.

The five most significant address bits ($A_5 - A_9$) also feed a decoder circuit that decodes the full 32 states. The outputs of the column decoder are used to control the switch transistors that connect the data lines of each memory cell to the sense amplifier for read operations or the write amplifiers for write operations. These transistors (Q_7 and Q_8 in

and one column is enabled. A si
memory selected is at the inter
addressed row and column. Wh
addressed, data can be read fro
into it as described before.

Another popular static memo
is the 256 × 4. This 1*k* (1024 b
also organized into 32 rows an
However, the circuits are arra
they can store 256 four-bit wo
address is needed to access 256 wo
The five least significant addres
to enable the 32 rows as in the 1
The three most significant ad
used to enable the selected colu
32 columns in the matrix, but

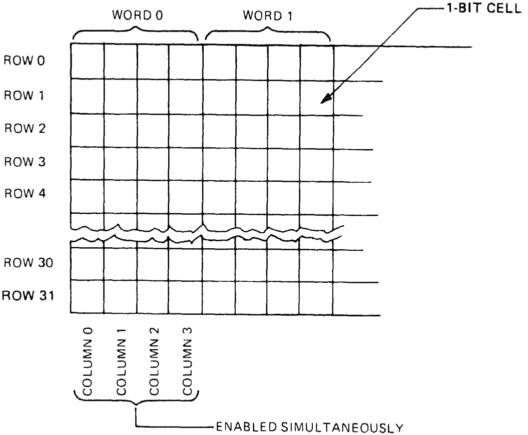


Figure 1-30.—Cell organization in a 256 × 4 static memory.

memories are also available. These memories are capable of storing a maximum of 4096 bits of data. Typical memory organizations are $4k \times 1$ or $1k \times 4$. These $4k$ memories are generally more desirable than their $1k$ equivalents. Higher density generally means less power consumption and lower cost.

Figure 1-31 shows how the $1k \times 1$ memory integrated circuits are used to construct a $4k \times 4$-bit memory system. It is made by interconnecting the $1k \times 1$ (2102) memory circuits into four groups of four circuits. Each 4-bit group can store 1024 four-bit words. To address a total of 4096 words, a 12-bit address word is used. The ten least significant bits of the address word are applied to all the memory

Dynamic Memories.—Becaus conductor memories are easy to u digital computer memory can be implemented very quickly with However, despite these benefits, st have a high cost per bit. This may in systems requiring extensive sto The primary cause for the high simply the relatively large amo required by the basic static cell. Si an integrated circuit is directly p the area of the silicon chip used, st are relatively expensive on a cost-

Another disadvantage of the s chip is its relatively high power When large storage capacity is re

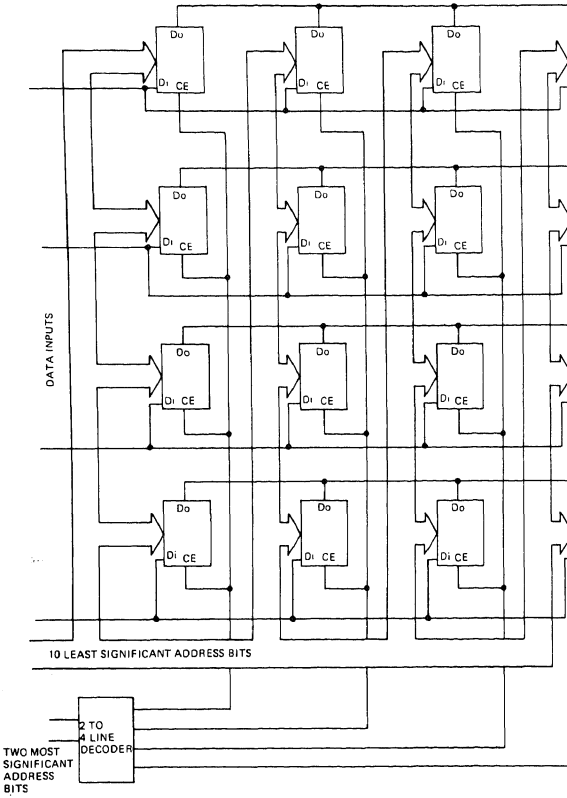

Do
Di
CE
DATA INPUTS
10 LEAST SIGNIFICANT ADDRESS BITS
2 TO 4 LINE DECODER
TWO MOST SIGNIFICANT ADDRESS BITS

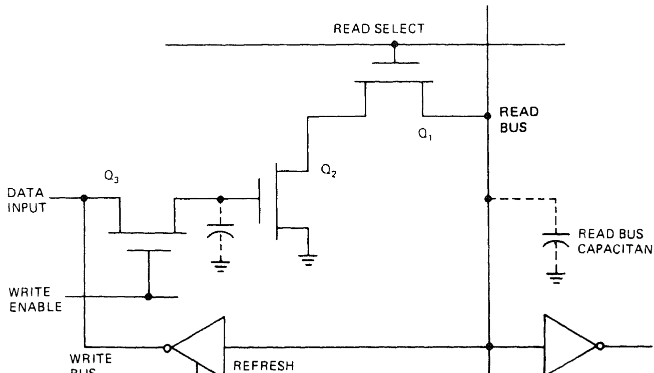
Figure 1-31.—A 4k × 4 static memory using 2102 static RAMs

necessary to restore the charge on the capacitor periodically to prevent the loss of the data. This process is called refreshing. Refreshing is performed during the time that a memory cell is being read and at a periodic rate determined by a clock oscillator circuit during the time the memory is idle. In most dynamic semiconductor memories, the memory cell must be refreshed every 2 milliseconds or more often to avoid the loss of data. Like a static memory cell, dynamic semiconductor memories are volatile since data will be lost if power is removed.

A basic three-transistor dynamic memory cell is shown in figure 1-32. This is the memory cell used in the type 1103 dynamic 1*k* × 1 memory. The storage element in this circuit is the gate capacitance of MOSFET Q_2. Q_1 and Q_3 are MOSFET switches that permit data to be written into and read from the memory element. To write data into the memory cell, the desired data is applied to the data input line. The write-enable line is then strobed, activating Q_3. Q_3 conducts and connects the binary logic level of the input to the gate of Q_2, charging or

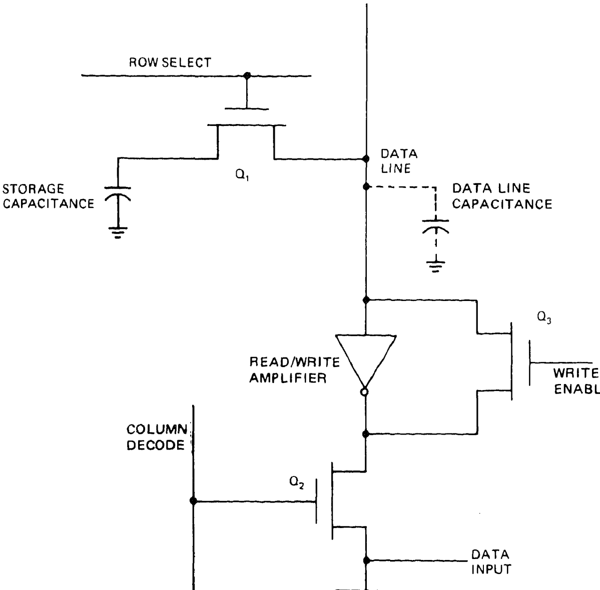
the read bus is precharged. This is
charging the capacitance on the
predetermined voltage. Next, the c
by the row address decoder when
read select line and activates Q_1.
switch that connects Q_2 to the r
binary 1 is stored in the cell, the ga
of Q_2 will be charged and Q_2 will
its low impedance will cause the pr
bus capacitance to be discharged.
the voltage on the read bus. This
level is then sensed by the out
which generates the appropriate lo
binary 0 is stored in the cell, the ga
of Q_2 will not be charged and
conduct. Its high impedance w
effect on the precharged read bu
Therefore, the voltage on the rea
be reduced significantly from i
value. The output amplifier then
appropriate output logic level for

Because of the small value
capacitance of Q_2, and the leakag
that device, the charge on the st



capacitance will leak off after a short period of time. Typically, if the charge on the capacitor is not refreshed every 2 milliseconds or more often the data in the cell will be lost. This refresh operation is accomplished by first reading the data out of a cell and then writing it back in. The refresh operation for the cell in figure 1-32 is started by recharging the read bus. The read select line is then enabled, turning on Q_1. The state of the read bus then reflects the charge on the gate capacitance of Q_2. The read bus drives the output sense amplifier as well as a refresh amplifier. During the refresh cycle, the refresh
amplifier is activated, placing
memory cell on the data input
enable line is then strobed, c
level on the output of the write b
in the gate capacitance. A clock
dynamic memory system autom
the refresh cycle to ensure th
stored in the memory remains
dynamic memory cells the refres
takes place during a read opera

Another widely used dynami
the single transistor cell shown
This storage cell consists of



capacitor and one MOSFET. Because of the simplicity of this memory cell, very high density memory circuits are possible. This type of memory cell has enabled semiconductor designers to put as many as 16,384 (16*k*) bits of storage circuitry on a single silicon chip. The cell in figure 1-33 is widely used in 4*k* and 16*k* semiconductor RAMs. The cell occupies an area about half that of the dynamic cell shown in figure 1-32.

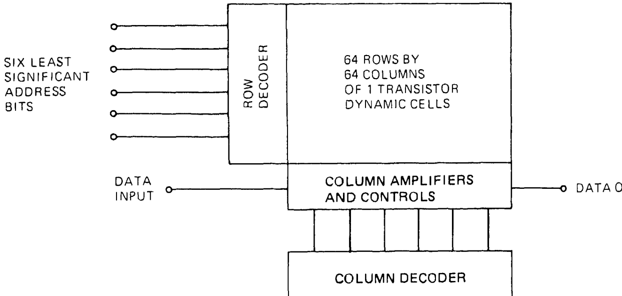
The row select line is enabled by the output of the row address decoder to read the data stored in a single transistor cell. This signal turns on the transistor in the storage cell (Q_1) connecting the voltage stored in the cell capacitance to the data line. This causes the data-line capacitance to be charged or discharged to a voltage determined by the relative sizes of the storage-cell capacitance and the data-line capacitance. The voltage on the data line is amplified by the read/write amplifier to the sense amplifier. The sense amplifier generates the appropriate binary logic output state.

The binary logic level to be stored is applied to the data input line to write data into the storage cell. The row and column decoders

enable transistors Q_1 and Q_2. T
line is then strobed turning on (
on the data-input line is then c
storage-element capacitance th
and Q_1, charging or discharging
by the input state. The read/wr
bypassed at this time.

The refresh operation is accor
ically and during read operatic
Q_3. This causes the output of
amplifier to be connected back
either charging or discharging t
accordance with its previous sta

Figure 1-34 illustrates how the
cells are organized to form a pra
ductor 4*k* × 1 RAM. Here, 409
cells are organized into a 6
Twelve address bits are required
4096 bits. Six address lines are c
row decoder which selects one o
matrix. The other six address
column decoder which selects one
The selected bit can then be read
into as described before. The refr
generally is accomplished on a
During refresh, an entire colu


SIX LEAST SIGNIFICANT ADDRESS BITS
ROW DECODER
64 ROWS BY 64 COLUMNS OF 1 TRANSISTOR DYNAMIC CELLS
DATA INPUT
COLUMN AMPLIFIERS AND CONTROLS
DATA O
COLUMN DECODER

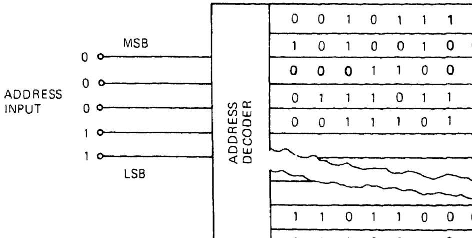
elements is refreshed simultaneously. A clock and counter sequentially enable the columns one after the other and refresh them to retain the data stored there. To reduce pin count in some dynamic RAMs, the address lines are multiplexed. Only six address lines are brought out to pins. This means that the six least significant address bits are loaded, then the six most significant address bits are loaded. On-chip storage registers hold the address bits.

READ ONLY MEMORIES (ROMs).—A ROM is a digital circuit used to permanently store binary information. Practical ROMs are available for storing as many as 65,000 bits of data. Most ROMs are organized into many storage locations for equal-length multibit words. For example, a typical 256-bit ROM might be organized into 256 storage locations for 8-bit words.

The main distinguishing characteristic of a ROM is that binary information is permanently stored there. The data is written into the memory when it is manufactured or, in some cases, after it has been manufactured. Unlike the read/write memory, data cannot be written into a ROM under program control. Data can be read only from the memory. Like read/write semiconductor memories, ROMs are also random-access memories (RAMs). Wh
to as RAMs, data in a
random, meaning that t
in the memory is the sa
word.

ROMs are widely
logic functions. A RO
replace many different t
random-logic circuits.
replace multi-input/mu
and are also used to p
and arithmetic operatio
the ROM offers the a
easier design, lower
often lower power con

While ROMs are of
conventional logic circu
tion in digital compute
storing programs and
stored in the ROM, the
and the digital comp
operation specified by
commonly used mem
system is a ROM where
to perform a specific f
used with a general-p
such as a microprocess
purpose digital compu



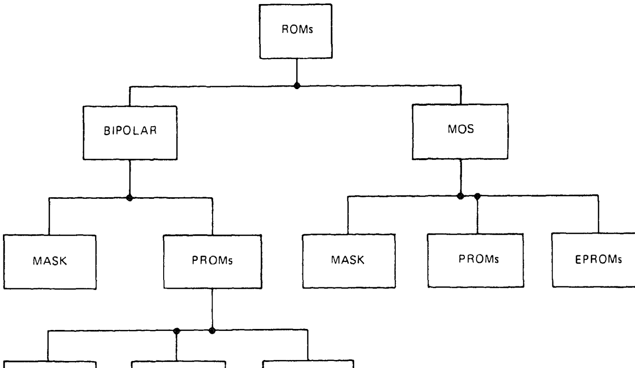
circuits. The address decoder monitors a multibit binary input word and decodes all possible states. Only one of the decoder outputs is activated and enables one of the word locations in the memory. As in other memory systems, the number of address input bits determines the number of memory locations. For example, if a 5-bit input word is used, a maximum of $2^5 = 32$ individual memory locations can be addressed.

The main body of the ROM consists of the electronic components or circuits that store the binary data. These storage elements are arranged as equal-length multibit binary words. For example, the memory shown in figure 1-35 is capable of storing 32 eight-bit words. The decimal addresses are designated 0 through 31. When a 5-bit address word is applied to the input, the contents of the addressed memory location will appear at the output. In figure 1-35, the address input is 00011, meaning that the contents of memory location 3 (01110110) will appear at the output. All other memory locations are disabled at this time. The output circuits buffer the memory contents from the storage elements and make the output signals compatible with other

Some ROMs are organized as
storage elements similar to that us
For example, a 1*k* ROM would be
a 32 × 32 matrix. Unlike RAM
multiple bits must be addressed in t
accomplish this, you must enable o
selects several memory locations
enable multiple columns to read c
word. For example, in a 32 × 32 bit
the 32 storage elements in a ro
organized into four 8-bit words. To
desired memory location, you would
of the desired columns simultane
column decoder.

Types of ROMs.—There are m
ways to implement ROMs. A variety
components and circuits can be u
binary data. For example, magne
capacitors have been used in this
However, most modern ROMs use s
components and circuits. A variety o
and circuit types are used.

Figure 1-36 shows a chart of th
types. The two major types of ROM



and MOS. Bipolar ROMS use bipolar transistors and, therefore, are capable of very high access speeds. Most bipolar ROMs are made with TTL or Schottky TTL circuits. The primary advantage of the bipolar ROM is its extremely high speed. Typical access times are about 20 to 90 nanoseconds. The access time of a ROM is the time between the application of the address input and the stable appearance of the output word.

MOS ROMs are more widely used than bipolar ROMs. MOS construction produces ROMs with higher density, lower cost, and lower power consumption. Both p- and n-channel types are used. The n-channel types are faster and can be constructed with higher density, thereby making them the more popular of the two types. However, MOS ROMs are slower than their bipolar equivalents. Typical MOS ROM access times vary from 400 nanoseconds to 1 microsecond.

As you can see in figure 1-36, both bipolar and MOS ROMs are further classified as mask ROMs or PROMs. A mask ROM is one in which the data is permanently stored during manufacture. The information to be written into a ROM is known prior to manufacturing. A special diffusion mask is constructed to reflect this information. This mask is then used in providing the proper diffusion patterns during the manufacturing process. Mask ROMs are the most economical type and are preferred for large-volume applications. However, the data must be known ahead of time and cannot be changed.

Another type of ROM is the PROM or programmable read-only memory. This type of ROM is manufactured by storing all binary 1s or all binary 0s during manufacturing. It is programmed in the field with a special programming device called a PROM burner or PROM blaster. In the case of a bipolar ROM, the programming is accomplished by "blowing" a fuse in the circuitry. A tiny fuse made of silicon or nichrome is placed at each bit location. The bit is programmed with a binary 1 or

it is manufactured. However, it h
advantage that the data stored in
can be erased and new informatior
basic storage element in an EPROM
with a floating gate element. The N
be turned on or off by applying a
voltage which charges or discharges
erase the PROM, the storage element
to ultraviolet light of the correct
and intensity. Most EPROMs are r
package that has a quartz winc
which the ultraviolet light can be p
this type of ROM is more expens
other types, the ability to reprogra
makes it highly desirable in developr
tions where programs and data m
changed to achieve the desired res

Typical ROM Circuits.—One o
and widely used types of ROMs
matrix ROM. It consists of a decod
of diodes where the presence or
diode in the matrix determines whe
1 or a binary 0 is stored. A simple
ROM is shown in figure 1-37. Th
store eight 4-bit words. A 1 of 8 de
selects the desired memory locat
binary input address determines
eight locations is read out. The
lines can be connected to the de
lines through diodes. Pull-up resis
on each of the four output lines.

To see how the diode matrix
let us assume that the decoder ha
outputs, that is, all outputs are
for the selected output, which
example, if the input address word
decoder output will be low wh
decoder outputs will be high. Th
cathode ends of the diodes associa
#4 output to be brought low.
conduct through their pull-up resi
example, A, B, and D will go low.

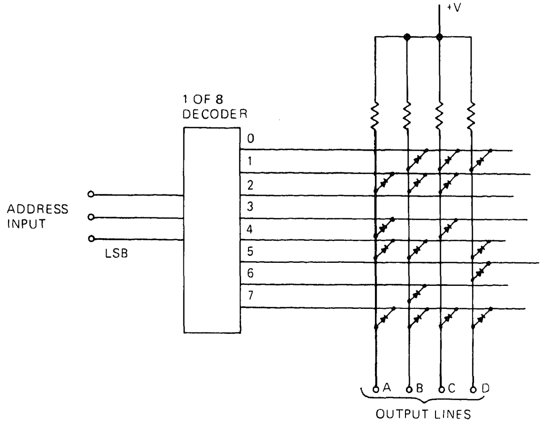


Figure 1-37.—Diode matrix ROM.

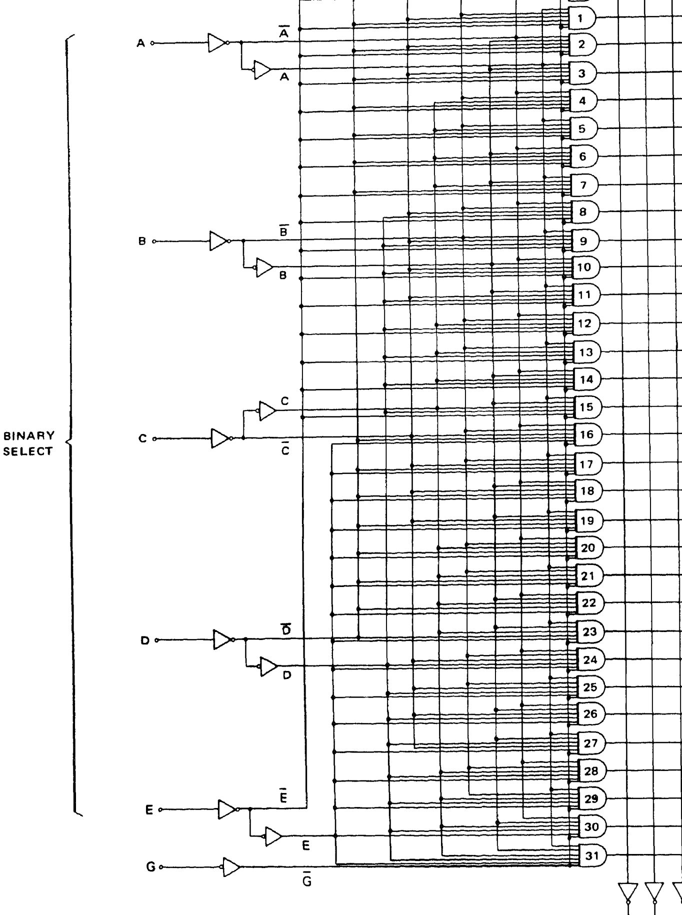
are also available. When the IC matrix ROM is made, diodes are formed at all possible memory locations, meaning that the memory is initially programmed with binary 0s. To store data in the memory, a high external current pulse is applied to the output lines so that specific diodes are reverse-biased and destroyed. By destroying a diode, it becomes open and a binary 1 state is programmed.

Figure 1-38 shows a typical programmable bipolar memory. This ROM uses TTL circuitry and is organized as 32 eight-bit words. The five input address bits are labeled A through E. The binary code applied to these lines will select one of the 32 eight-bit words stored in the memory. Most of the circuitry is a 1 of 32 decoder circuit. Eight output buffer circuits interface the ROM

connections are made through pr
links which can be of the fuse or m
an emitter from the decoder is con
input of an output buffer through
output voltage will go low (binary
decoding gate is addressed. Leavin
from the input buffer open progran
A high-output voltage will be read
associated buffer decode gate is ac

Note that the output buffe
collector transistors which can be
parallel to expand the size of t
Three-state output buffers are a
some ROMs for the same purpose

MOS ROMs are more widel
bipolar ROMs because of the highe
lower power consumption of the


BINARY SELECT
A
$\overline{A}$
A
B
$\overline{B}$
B
C
C
$\overline{C}$
D
$\overline{D}$
D
E
$\overline{E}$
E
G
$\overline{G}$

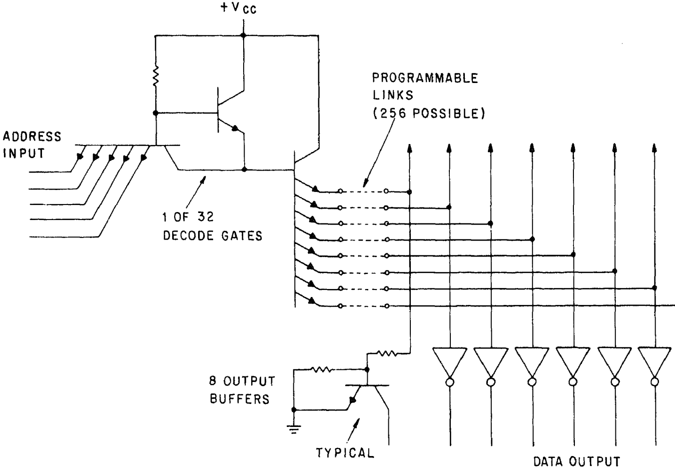
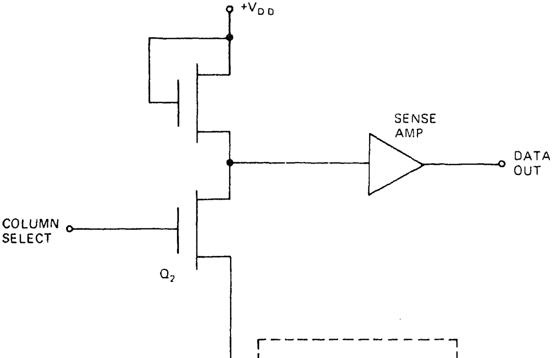
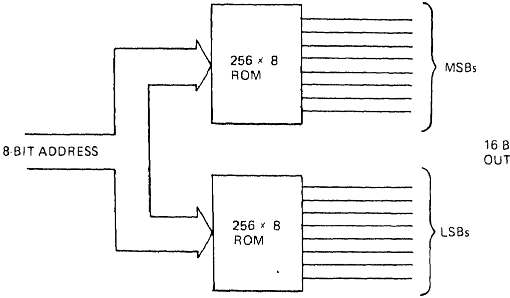


Figure 1-39.—Typical TTL ROM cell.

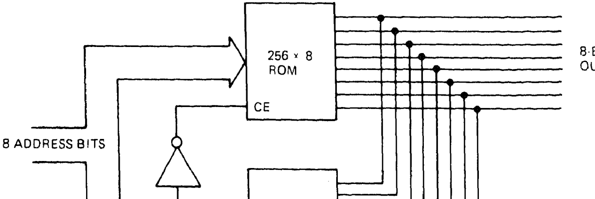


and column decoders interpret the input address and select the desired memory location. The storage element in this circuit is MOSFET Q_1. The gate of the storage element is enabled by the output of the row select decoders. If Q_1 is present and the row select line connected to its gate is enabled, Q_1 will conduct and bring the bit line low. This low state may or may not be fed to the output sense amplifier, depending upon the state of Q_1. Q_2 is a MOSFET switch enabled by the column decoder. If Q_2 is selected, the decoder output will turn it on and connect the state of Q_1 to the output sense amplifier. If Q_1 is not present, the bit line will essentially be open. When Q_2 is selected, the open state will be
by the sense amplifier. As we
for a MOS ROM, only one row
enabled at a time. However, r
are enabled to read out a mult

Figure 1-41 shows two way
conductor ROMs can be interco
larger memories. In view A, two
are connected to form a 256
memory. Note that the address li
in parallel. Two 8-bit words
simultaneously with this arrang
significant 8 bits of the 16-b
are stored in the upper ROM
significant 8 bits are stored
ROM.



VIEW A



Another typical memory organization is shown in view B of figure 1-41. Here, the two 256×8 memories are connected to form a 512×8 memory. Nine address bits are needed ($2^9 = 512$). The most significant bit (ninth address bit) is used to control the chip enable (CE), sometimes referred to as a chip select, inputs on the ROM. An inverter is used to make the chip enable to each ROM complementary. The remaining eight bits are common to both memories. With this arrangement, the lower 256 words (locations 0 to 255) are stored in the lower ROM while the upper 256 words (locations 256 to 511) are stored in the upper ROM.

The ROM outputs are connected in parallel. They must be either the open collector or three-state type for this arrangement to work. When the ninth address bit is low, the lower ROM is enabled. The inverter causes the upper ROM chip select input to be high, thereby disabling it. All outputs of the upper ROM will be high if open collectors are used or will be in the high-impedance state if three-state outputs are used. The unused ROM has no effect on the output signals. Additional ROMs may be connected in parallel to form even larger memories. External gates may be required to decode the additional address input bits to operate the chip-enable lines.

INPUT/OUTPUT (I/O) SECTION

The I/O section is that portion of the digital computer through which the CPU communicates with the external peripheral devices. In a useful computer function, data is read into the computer, processed, and then transferred to the output. The peripheral units handle the data input and output display functions. The I/O section controls the transfer of data between the computer and the peripherals.

The I/O section is the interface between the computer and any external devices. An interface is an assembly of electronic circuits that make

required to properly interface differ
logic circuits. For example, logic-lev
often required to properly interface
MOS circuits. The speed of the data
must also be compatible. Some type
storage between the two units may
as a buffer to match the high-spee
low-speed peripheral unit.

Control is another function of t
There are status lines that tell when t
or peripheral unit is ready or bus
lines that actually initiate the da
This process is often referred to as h

The type of information exchan
the I/O unit and the peripheral dev
data, addressing, and control si
multiple I/O units can usually be co
computer, some coding scheme is
select the desired unit. This is usual
a binary word used as an address. T
transmitted to all the peripheral
unit recognizing the address is conn
I/O section. Data can then be trans
from the device over the intercon
lines. The actual data transfers are c
control signals between the two de

Programmed data transfers tha
as the result of executing an I/O
usually cause data to be transferred
peripheral unit and the accumulato
the CPU. Other CPU registers may
depending upon the computer arch
the instruction. In some computers
units are treated as memory loc
peripheral units are addressed as s
tions and all memory reference inst
be used in performing I/O ope
special I/O instructions are used.

Parallel vs. Serial Data Transmissi

There are two methods of
digital data: parallel and serial. In
transmission all bits of the binary da

and expensive. This is particularly true if the distance between the two units is great. Long multiwire cables are not only expensive but also require special interfacing to minimize noise and distortion problems.

Serial data transmission is the process of transmitting binary words a bit at a time. Since the bits time-share the transmission medium, only one interconnecting lead is required.

While serial data transmission is much simpler and less expensive because of the use of a single interconnecting line, it is a very slow method of data transmission. Nevertheless, serial data transmission is useful in systems where high speed is not a requirement. Serial data transmission techniques are widely used in transmitting data between a computer and its peripheral units. While the computer operates at very high speeds, most peripheral units are slow because of their electromechanical nature. Slower serial data transmission is more compatible with such devices. Since the speed of serial transmission is more than adequate in such units, the advantages of low cost and simplicity of the single interconnecting line can be obtained.

Noise and Distortion

The primary function of the data transmission medium is to carry the electrical signals reliably from one location to another. If transmission lines are used, they must introduce a minimum of noise, loss, and distortion. The greater the transmission distance, the greater the chance for data errors because of these factors.

Noise is any electrical interference that can cause errors in the data transmission. Noise in a digital system takes many forms. It can be cross talk from signals in adjacent paths. High-speed logic signals are easily coupled, inductively or

generate transients and ha
affect the operation of
quality, low-impedance
grounding systems, and a
can greatly minimize suc
can also be overcome by
high noise immunity, se
conductors to minimiz
keeping all interconn
minimize inductance a
avoiding long parallel
cable.

Transmission lines al
current resistance dro
significantly reduce the
mitted signal, thereby lov
ratio. Such losses are m
transmission lines as sh
using low-resistance cab

Distortion is anothe
duce errors in data tran
the binary pulses is cause
capacitance of the tr
reactive components for
rounds off pulses and
time. The phase shift or
line further distorts the p
minimized by using hig
and high-powered line

Line Drivers and Recei

A line driver is the lo
the desired binary signa
line. Line drivers are a
For short transmission
feet, most standard log
line drivers. However,
used, special line drive
The high capacitance of

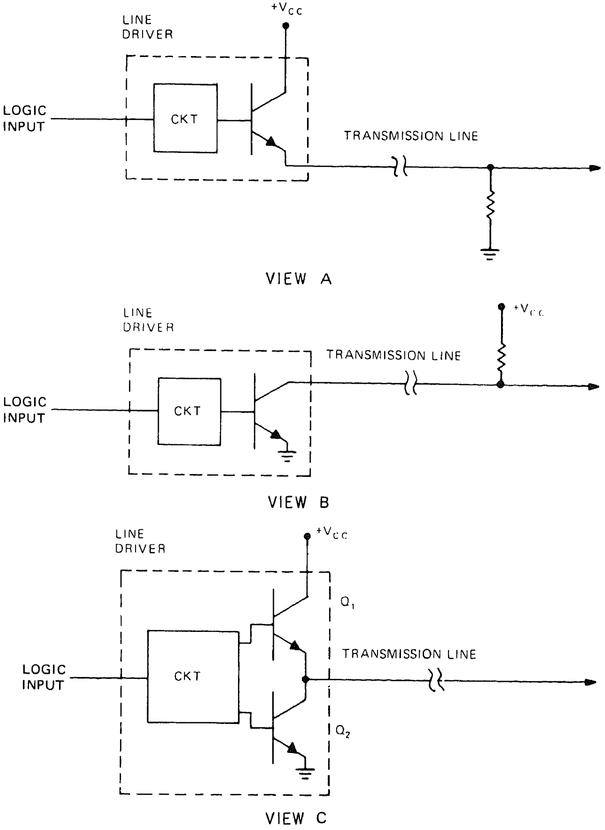


Figure 1-42.—Type of line drivers. (A) Emitter-follower; (B) inverter; and (C) totem pole.

and Q_1 is on. Properly designed totem pole circuits can drive a significant amount of cable capacitance at high speeds. Three-state versions of the totem pole line driver are also available for operating long cables in bus-oriented systems. All the line drivers described here can generally furnish as much as 100 milliamperes of current to a transmission line.

Line receivers are the logic circuits at the opposite end of the transmission line. A line receiver looks at the logic signal being transmitted down the transmission line. Its primary function is to discriminate against any noise picked up on the line, reshape the logic signal caused by line distortion, and generate logic signals compatible with the logic circuitry at that end of the line.

In its simplest form, a line receiver is simply a logic gate. For short transmission lines, standard logic gates have sufficient noise immunity to be used adequately as line receivers. However, when transmission lines become more than several feet long, special linear and digital line receivers should be used for best results.

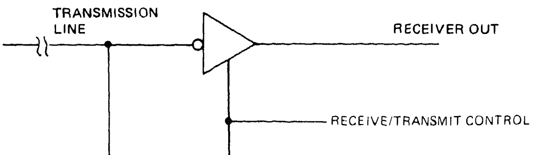
A widely used type of line receiver is the Schmitt trigger. It is used because of its built-in hysteresis and high noise immunity. The Schmitt trigger is basically a bistable circuit whose state is a function of its input voltage level. The output logic state of the Schmitt trigger changes

if the input signal passes throu
lower input voltage thresholds. I
high input voltage to overc
threshold of the Schmitt trig
this, low-level noise signals a
effectively filtered out. Only th
voltage transients are recogniz

Another type of line receive
amplifier connected as a compa
comparator inputs is a fixed-
sets the input voltage threshol
noise immunity of the circuit.
trigger, a line receiver with an
does not recognize low-level n
below its threshold. Only the
logic signals are recognized.
receiver provides high noise im
amplification.

A desirable characteristic o
is high-input impedance. This
of the transmission line and al
to terminate the transmission li
istic impedance. As long as the
of the receiver is about 10 time
characteristic impedance of th
loading will occur.

Often the functions of a
receiver are combined in a
circuit package. Such circu
known as transceivers. (See fi



bidirectional; that is, the same line is used to transmit data in both directions. When the line driver is sending data, the receiver is disabled. When the line receiver is being used, the line driver is disabled. A receive/transmit control line is used to determine the mode of the circuit. A typical line transceiver IC contains four identical transceiver circuits. Schottky three-state TTL circuits are widely used.

Parallel Data Transmission

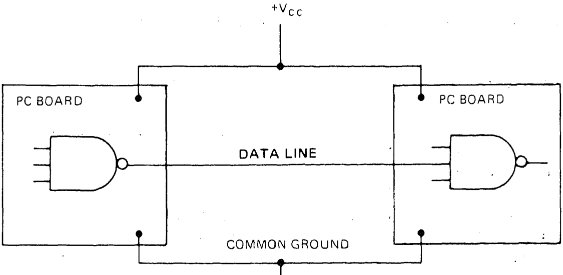
In a parallel data transmission system, each bit of the binary word to be transmitted must have its own data path. There are a variety of ways to implement this data path. The two basic classifications of transmission line circuits are single-ended and balanced. Single-ended transmission systems use a single wire data path for each bit. When combined with a ground or return reference, the electrical circuit between the sending circuit and the receiving circuit is complete. In a balanced-transmission line system, two conductor cables are used to send the data. The data on the dual-transmission line is complementary. The dual-transmission lines also use a ground return reference. While a single-ended transmission line is simpler and less

SINGLE-ENDED TRANSMIS
TEM.—The simplest connection
made between two circuits is a
Figure 1-44 shows a single-wire in
between two circuits on two ad
boards. The interconnecting line c
the common ground forms the
path.

For such a simple transmission
properly, the distance between the
receiving circuit must be as short
For high-speed TTL and ECL c
6 inches maximum is recommende
speed operations with TTL circu
connecting line of up to 5 feet n
successfully in some applications.
long distance communications b
circuits, other methods must be u

The reliability of data transm
improved by using a two-wire syste
transmission lines can take severa
of the wires is the data path wh
is the common ground reference. T
basic double-wire types commonly
include the parallel double-wire,
pair, and the coaxial cable.

The simplest form of double
mission systems is the dual-paral



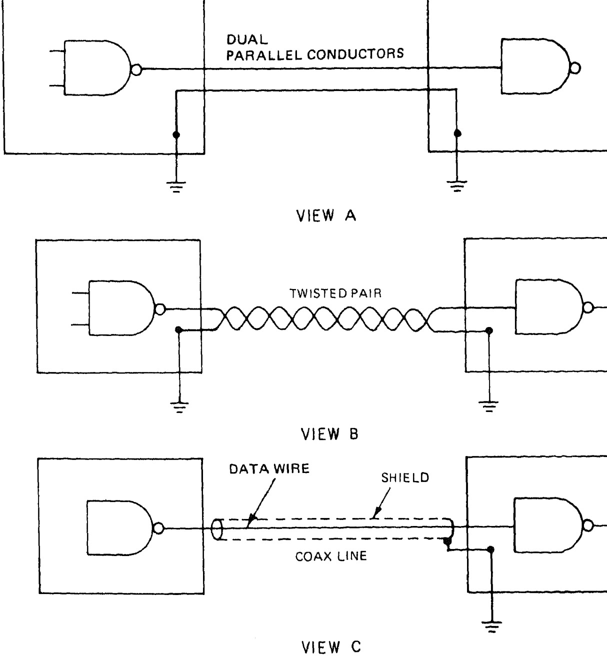


Figure 1-45.—Single-ended transmission lines. (A) Dual wire; (B) twisted pair; and (C)

shown in view A of figure 1-45. A single dual-parallel conductor cable is used for each bit to be transmitted. The closely adjacent ground helps minimize noise pickup. Such parallel conductors are often implemented as multiple dual connections within a single flat cable. Multiple wires or insulated conductors are

type of ribbon cable is thin convenient in interconnecting parallel data paths. Ribbon called stripline.

Another commonly use mission line is the twisted pa

The best dual-line transmission system for single-ended systems is the coaxial cable shown in view C of figure 1-45. Here, the data line is shielded by a coaxial braid. A coax cable provides better shielding against noise than the twisted pair or the parallel double line. Note that the shield is usually grounded only on the receiving end of the line. Coaxial cable is a transmission line and, therefore, must be properly terminated for proper data transmission. Characteristic impedances of 50 to 200 ohms are commonly used in digital data transmission. Despite the high noise immunity of coaxial cable, it does have relatively high losses requiring high drive voltages and currents for good transmission. It is also the most expensive of the three types of single-ended transmission lines.

BALANCED TRANSMISSION SYSTEMS.—Balanced-line transmission systems use two conductors for each bit to be transmitted in addition to a common ground. The signals on the two lines are complementary. The line drivers have two complementary outputs while the receivers are usually differential amplifiers.

Line drivers for balanced-line systems are similar to those for single-ended systems, except that two complementary outputs are required. Two of the line-driver circuits shown in figure 1-42 can be used to drive each line in a balanced-transmission system if the inputs to these drivers are complementary. An inverter is used to provide the complement logic signal.

A differential line receiver has two inputs, one from each side of the balanced- or dual-transmission line. The input circuit to most differential line receivers is a diffe fier. The complementary logic s input line cause the differential generate a large voltage swing which is then translated into the voltage levels. However, any noise the transmission line will be co that is, the same noise will be both wires. These equal noise si applied to the differential inputs o Because of the common mode reject istics of the differential amplifie signals will be effectively balanced transmission line systems depend on mode rejection characteristic, shielding, for noise elimination.

As in single-ended systems, thr of transmitting cables are used systems. These are the dual wir pair, and the coaxial cable. The du is used at low frequencies where short. Two loose or parallel wires such applications. Such means of in are usually limited to distances le 3 feet.

Figure 1-46 shows a typical ba mission line system. Twisted-pair so that noise induced into the line same effect on both wires. The lov cost of this cable make it a popu data transmission line for balanced shielding provided by coaxial cable required since balanced transmi depend upon common-mode charac than shielding to minimize noi environmental noise levels, shie pair cables are available.

shield are also available for balanced-line transmission systems. Such cables are used where extreme noise problems are encountered. The disadvantage of coaxial cable compared to twisted pair is its high cost, weight, and great loss.

Serial Data Transmission

The simplest, most economical, and easiest to use method of transferring digital information from one point to another is serial data transmission. In a serial system, the digital data is sent one bit at a time; therefore, only a single pair of transmission wires is required. The serial transmission of data is far slower than parallel transmission. However, in most computer systems the low-speed penalty is no disadvantage. Data rates achievable in serial data systems are sufficiently high to make them very practical.

Serial data transmission is preferred because it is inexpensive. It is especially beneficial in transferring data over long distances. For long distances, you can see that multiple parallel lines are far more expensive than a single cable.

Low-speed serial data transmission also offers another benefit; that is, the data rates are slow enough to permit the transmission of data over telephone lines. In this case the digital data is converted into a pair of audio tones representing binary 1s and 0s. These can be transmitted very economically for long distances over standard telephone lines. In addition, low cost tape recorders can be used to record the serial data. This provides a low-cost means of mass data storage and retrieval. Standard audio cassette recorders are widely used in this application.

Serial data transmission also permits transmission of data by radio. A radio communications path represents only a single interconnecting link similar to a transmission line pair. Therefore, for data to be transmitted by radio it must be in

There are several different
mitting serial data from one
These methods are classifiec
directional nature of the trans
of the transmission, and the
senting binary data. Let's cor
methods.

The two terms that descr
characteristics of serial dat
simplex and duplex. A simpl
which serial data is transmitt
only. If communications in l
required, two transmission l
direction, are required. Sin
systems are not widely used b
of a bidirectional capability.
find special applications wh
transmission is required.

The most commonly use
data communications is by the
duplex system, serial data ca
one direction or the other ove
sion line pair. When data is tra
direction and then the other,
half duplex. Data cannot be t
directions at the same time ir
tem. A full-duplex system is or
be transmitted in both directi
on the same transmission lin

Another method of clas
communications is by the ti
The two basic types of ti
synchronous and asynchronc
system is one in which all dat
step with a master timing sigr
systems, a clock oscillator is
data transfers and other opera
systems are difficult to u
transmission because of the
path. Normally, both the da
timing signal must be trans
synchronization at the receivi
the problems involved with sy

The most widely used measure of speed is the baud rate. The baud rate is a measure of the number of times the signal changes per second. One baud is one binary level change per second. The bit and baud rates can be equal if a series of alternating 1s and 0s is taking place.

The baud rates for serial data transmission have been standardized for most computer applications. Typical popular baud rates are 110, 300, 600, and 1200. Baud rates of 2400, 4800, and 9600 are also used in high-speed systems. Rates of 110, 300, and 600 baud are widely used with cathode ray tube (CRT) terminals.

Binary format is another characteristic of serial data. Binary data can be transmitted as voltage or current levels or by dual-audio tones. Regardless of the method used in serial systems, a binary 1 is referred to as a mark and a binary 0 is called a space. Standard TTL voltage levels are widely used in transmitting serial data. TTL-compatible voltage levels fix the binary 0 level between 0 and +0.8 volts, while a binary 1 is between +2.4 and +5 volts.

Serial data can also be transmitted by two different current levels. A commonly used standard is 20 milliamperes used in communication with the Teletype ASR-33 terminal. Here, a

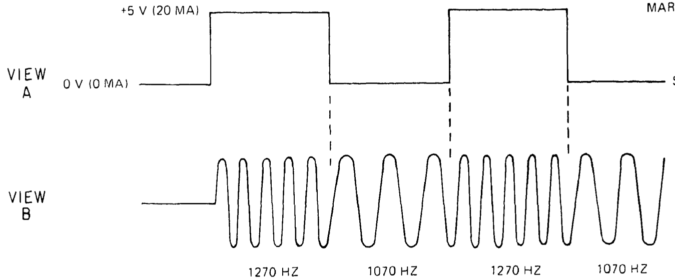
transmitted over long distances (u
more) with little loss in transmissi
interference from noise. Both th
voltage formats are shown in vie
1-47.

Another method of transmittin
is by the use of audio tones. A bin
mitted as one tone while a binary 0
as another tone. This method of se
mission is called frequency shift ke
is widely used to transmit data over
by use of telephone lines. FSK seri
easily recorded on magnetic tape

Standard audio tones have be
for use in serial data transmission
example, in transmitting data o
lines, the following binary 1 and
quencies are used:

Binary 0 = space = 1070
Binary 1 = mark = 1270
Binary 0 = space = 2025
Binary 1 = mark = 2225

View B of figure 1-47 shows a
signal.



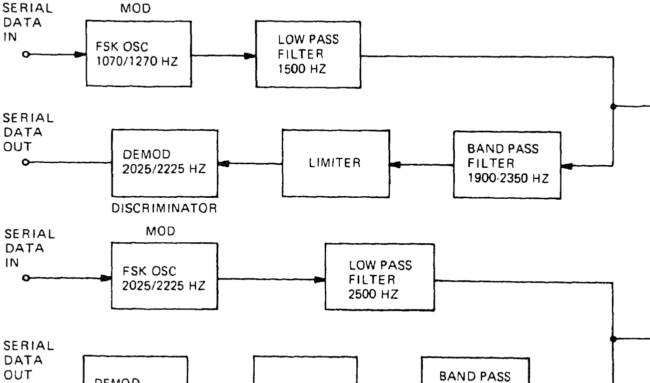
single transmission line. This is the method used in full-duplex operations. Data can be sent from one source to another in one direction by the use of the 1070- and 1270-Hz signals. Filters are used to separate the signals.

The units that are used to send and receive FSK serial data are called modems, meaning modulator-demodulator. For full-duplex operation, a modem is required at each end of the transmission line. Figure 1-48 shows a block diagram of a modem used to send and receive FSK data using the frequency standards given above. By referring to the figure, you can see that the serial data to be transmitted is applied to an oscillator whose frequency can be shifted (modulated) by the binary input. The oscillator applies the 1070 and 1270 sine-wave audio tones to the transmission line. This modem receives binary data at the higher frequencies. A filter selects the signal, limits its amplitude, and demodulates it. The demodulator is a frequency discriminator that generates a binary 1 or

transmission line is send
2225 Hz. The receiving p
demodulator or discrimin
transmitted at the lower

When the binary da
radio, different audio fr
binary 1 and 0. Typical fr
purpose are 2125 Hz for
and 2925 Hz for a spac
audio tones can frequenc
late a carrier to transmit
discriminator on the rece
two audio tones into bin

The most common m
serial data is to use t
Standard Code for Inf
(ASCII) code. See figure
(binary, BCD, and so fo
into ASCII characters. M
computer exists as paralle
data conversion is first pe
to-serial conversion is
receiving end, the serial A



0000	NUL	DLE	SP	0	@	P	\	P
0001	SOH	DC1 ENTER	!	1	A	Q	a	q
0010	STX	DC2	″	2	B	R	b	r
0011	ETX	DC3	#	3	C	S	c	s
0100	EOT	DC4	$	4	D	T	d	t
0101	ENQ	NAK	%	5	E	U	e	u
0110	ACK OFF-LINE	SYN	&	6	F	V	f	v
0111	BEL	ETB (XMIT)	′	7	G	W	g	w
1000	BS	CAN	(	8	H	X	h	x
1001	HT	EM	)	9	I	Y	i	y
1010	LF	SUB	*	:	J	Z	j	z
1011	VT	ESC	+	;	K	[	k	{
1100	FF	FS	,	<	L	\	l	¦
1101	CR	GS	—	=	M	]	m	}
1110	SO	RS	·	>	N	Λ	n	∽
1111	SI	US NEW LINE	/	?	O	—	o	RUB OUT

Figure 1-49.—ASCII code chart.

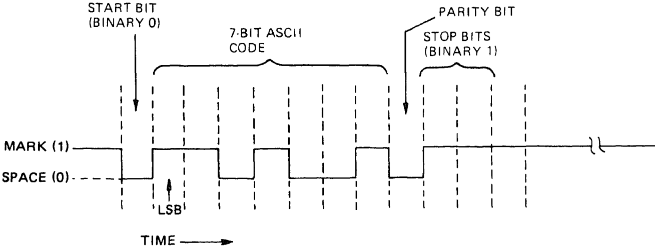


Figure 1-50.—Format for a serial data word using ASCII code for letter K.

at the binary 1 level. When a data word begins, a start bit occurs. The start bit is a binary 0. This binary 1 to binary 0 transition signals the beginning of a word. Following the start bit are the 7-bit ASCII code bits. The least significant bit (LSB) is transmitted first. Each bit can be either a binary 1 or a binary 0 depending upon the character or control signal transmitted. The letter K is being transmitted in figure 1-50. After the seventh ASCII bit, a parity bit is transmitted. The parity bit permits error checking in the system. Either odd or even parity can be used. Even parity (even number of binary 1s in the word) is used in figure 1-50.

Following the parity bit, two stop bits are transmitted. A stop bit is a binary 1 level. Note that the time interval for the transmission of each bit is a fixed value depending upon the baud rate. The baud rate of 110 represents a bit time of 9.09 milliseconds. A 300 baud rate translates to a 3.33 millisecond bit time.

$$\text{Time for one bit (milliseconds)} = \frac{1000}{\text{baud rate}}$$

While the 7-bit ASCII code is the most widely used for serial data transmission, other codes can be accommodated. For example, 6- and 8-bit versions of the ASCII code are also used. In some older systems, the 5-bit Baudot telegraph code is sometimes used. In addition, the parity bit is usually optional. While the code format and parity bit may change, all serial data words must have at least one start bit and a stop bit for proper operation.

UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER.—The digital circuit used to send and receive serial data in a digital system is called a universal asynchronous receiver transmitter or UART.

The transmitter portion of the UART converts parallel data into serial data. In addition,

in a single 40-pin dual in-line pac

The transmitting and receivin
a UART are completely separate an
Therefore, the UART can send an
simultaneously. Figure 1-51 sho
diagram of a typical UART. The A
parallel input data to be transmit
to a holding register. The word i
register is then loaded into th
output shift register. A parity gener
to the holding register outputs
appropriate parity bit which is lo
proper position of the output shif
control circuitry in the UART al
start and stop bits. A clock signal
UART then causes the data to be
out of the shift register. The start
and is then followed by the dat
The rate of transmission is d
the clock frequency. For most UA
frequency is set to 16 times the
rate. For example, to obtain a 1
110 × 16 = 1760 Hz clock pulse

A variety of control input sig
determine the format of the wor
For example, the number of tra
bits (one or two) can be controlled
of the binary level on one contro
control signal on another line d
parity bit will be used. A third lin
odd or even parity if a parity bit i
additional control input lines a
binary code that determines the
binary character transmitted. Mo
transmit 5-, 6-, 7-, or 8-bit serial
the control input lines can be h
fixed format is being used. Othe
signals from switches can be used
mode as desired.

The following discussion ref
ceiver sections of the UART sh
1-51. The serial input data is a
receiver input register. A start de

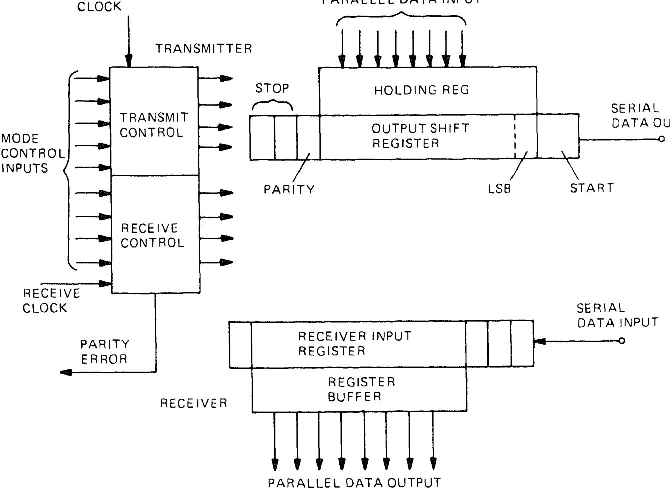


Figure 1-51.—Block diagram of a UART.

the circuit. The desired clock frequency is 16 times the baud rate as in the transmitter.

A parity detector circuit in the UART checks the parity of the received word and generates a binary output signal that determines whether a parity error has occurred. Stop-detection circuitry monitors the stop bits, then turns off the timing circuitry at the appropriate time in the reception of the transmitted word. The data word is then transferred into a receiver output buffer register. From there the data can be transferred to other parallel digital circuitry. The receive control circuitry sets up the receiver circuitry for the proper word format.

- Calculate the sum of the
  step 1.
- Compute the reciprocal of t
  step 2.

A general outline for calc
resistance of a parallel resistance ci
been derived.

The process of preparing a p
this explanation is not difficult
characteristic of the computer r
sidered: it cannot think. It can

follows: (Note: The instructions are read sequentially unless otherwise stated.)

- Locates parameters (constants) and such data as necessary for problem solution.
- Transfers the parameter and data to the point of manipulation.
- Performs the manipulation according to certain rules of logic.
- Stores the results of manipulation in a specific location.
- Provides the user with a useful output.

Even with a simple program, such as the resistance program, each step must be broken down into a series of machine operations. These instructions, along with the parameters and data necessary for problem solutions, must be translated into a language or code that the computer can understand.

Programming is a complex problem that may involve writing a large number of instructions. It may also involve keeping track of a great many memory cells that are used for instruction and data storage, which is time consuming and can lead to errors.

To reduce time and the possibility of errors for complex program preparation, the compiler has been developed. The compiler is a program that takes certain commands and then writes, in a form the machine understands, the instructions necessary for a computer to execute these commands. Compilers can bring many instructions into the final program when called upon or signaled by a single source statement. The compiler is problem oriented because the operations produced are those needed to work the problem as set out by the problem statement. Compilers are built at various levels or degrees of complexity. The simplest form of compiler

an assembler. Note th
opportunity to use the wr
(2) no necessity to conv
octal.

A more sophisticated
statement such as "mult
and generate all the inst
the computer to:

- Locate the factors
  the principal and
- Transfer these fa
  unit.
- Perform the indic
  tion (in this case th
  principal by the r
- Store the resultant
  be the interest or

The compiler also kee
allocations, whether be
instructions.

Depending on the cor
to be solved, programs m
a few instructions to man
tions. Ultimately, the pr
significant, perhaps even
of computer memory.
preclude this possibility
gram, storing seldom us
storage, and reading th
memory only when th
important method of de
through the use of subro

SUBROUTINES

As a program grows l
must be repeated. If the
to perform each of these

utine of the main program. Depending upon e complexity of the program, there may so be subexecutive routines within the executive utines.

Housekeeping is a term used frequently with broutines. At the time of entry into a sub-utine, the contents of the various addressable gisters may or may not be of value. An dressable register is defined as any register nose contents can be altered under program ntrol. The programmer must take steps to eserve the contents of these registers unless ey are of no value. This process is termed lousekeeping."

mp and Return Jump Instructions

The jump and return jump instructions are ed to facilitate construction of executive utines. These instructions provide the computer th the ability to leave the sequential execution the main program or executive routine, execute y of the subroutines stored in its memory, and en return to the execution of the main pro-am.

Execution of a return jump instruction uses the address of the next instruction to be ecuted in the main program to be stored sually in the entry cell of the subroutine). It en causes the instruction of the second cell of e subroutine to be executed. The last instruc-on to be executed will usually be a straight mp to the address contained in the entry cell. nce a jump instruction specifies the address of e next instruction to be executed, the computer provided with a means of returning to the main ogram once the subroutine has been executed.

ROGRAM CONSTRUCTION

The process of writing a program is broken

- Flow diagram—A flow diagr chart is an expansion of steps in which symbols are used to represent the operations to be performed and the s in which they are to fall. We will flow diagraming concepts later in t tion.

- Encoding—The process of conver operations listed in the flow chart into l the computer will use; either machine instr words, or compiler statements.

- Debugging—The process of errors in the program. Various tec are available for this purpose. A p may be written to include some aids f or a separate debugging program may b test the operation of a malfunctioning p For a simple program, a trial soluti be done on paper and the computed compared with those actually obtained step.

- Documentation—Documentation important because later changes may be w in a program or it may be desir use subroutines from another program. documentation will ensure that this accomplished. Documentation should i

  - Program title.
  - Problem statement.
  - Programmer's name.
  - Date.
  - Memory area used and/or nu cells used.
  - Registers used

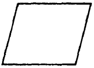
This map is commonly called a flow chart or flow diagram and serves a multitude of important functions. The flow chart "maps" the logical steps required, decisions to be reached, and paths to be followed as a result of the decisions. When properly annotated it defines input/output requirements, address allocations, data accuracy considerations, and register usage. A flow chart is valuable when "debugging" a program and when making future changes.

Flow charting can be constructed at various levels of complexity. A high-level flow chart consists of a few symbols and presents a broad overview of the problem. A low-level flow chart may approach a one-to-one correspondence between flow chart symbols and program instructions. Usually, there will be several flow charts for a program area. These may be compared to the prints found in a maintenance manual. Maintenance manual prints include a block diagram to show the relationship of the major units (high level), functional block diagrams showing the major circuits in a unit (intermediate level), and the schematics of the circuits (low level). Flow charts should be at such a level that they will implement all the uses previously discussed.

Flow Chart Symbols

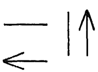
Symbols are used on a flow chart to represent the functions of an information processing system. These functions are input/output, processing, flow direction, and annotation.

BASIC SYMBOLS.—A basic symbol is established for each function and can always be used to represent that function. Specialized symbols may be used in place of a basic symbol to give additional information. The basic symbols are as follows:

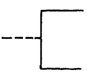


INPUT/OUTPUT SYMBOL. Represents any type of medium or data available for processing (input), or the processed information (output).

of value, form, or location of information.

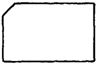


FLOWLINE SYMBOL. Normal direction of flow is from left to right and top to bottom. If the direction of flow is other than normal, arrowheads are required at the point of entry.

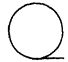


ANNOTATION SYMBOL. Used for the addition of descriptive comments or clarification notes. The broken line may be extended in whatever fashion to any symbol where applicable.

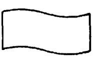
SPECIALIZED INPUT/OUTPUT SYMBOLS.—These symbols are used to construct all final programming flow charts. They more specifically define the medium on which the information is recorded or the manner of handling the information.



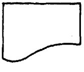
PUNCHED CARD SYMBOL. Used for an I/O function in which the medium is punched cards.



MAGNETIC TAPE SYMBOL. Represents an I/O function in which the medium is magnetic tape.

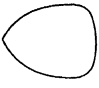


PUNCHED TAPE SYMBOL. Used for an I/O function in which the medium is punched tape.

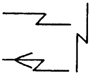


DOCUMENT SYMBOL. Represents an I/O function in which the medium is a document.

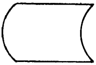
means of on-line keyboards, switch settings, and pushbuttons.



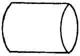
DISPLAY SYMBOL. Represents an I/O function in which the information is displayed for human use at the time of processing by means of on-line indicators, video devices, console printers, plotters, and so forth.



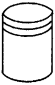
COMMUNICATION LINK SYMBOL. Denotes automatic transmission from one location to another. The direction of flow is left to right and top to bottom. Arrowheads are used when increased clarity is desired.



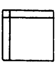
ON-LINE STORAGE SYMBOL. Indicates the use of a mass storage unit such as magnetic disks and drums.



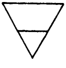
MAGNETIC DRUM SYMBOL. Represents an I/O function in which the medium is specifically magnetic drum.



MAGNETIC DISK SYMBOL. Represents an I/O function in which the medium is specifically magnetic disk.

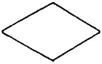


CORE SYMBOL. Represents an I/O function in which the medium is magnetic core.

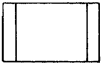


OFF-LINE STORAGE SYMBOL. Represents any off-line storage of cards, paper, and all other media.

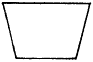
These symbols identify the specific type of operation to be performed on the information.



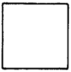
DECISION SYMBOL. Used to depict a point at which a branch or switching type of operation is possible to one of two or more alternate paths.



PREDEFINED PROCESS SYMBOL. Indicates a named process consisting of one or more operations or program steps that are specified elsewhere; for example, subroutine or logical unit. (Elsewhere means not in this set of flow charts.)



MANUAL OPERATION. Represents all manual off-line operations that do not require mechanical aid. These are clerical processes geared to the speed of the operator.



AUXILIARY OPERATION SYMBOL. Represents an off-line operation performed on equipment not under direct control of the central processing unit.

ADDITIONAL SYMBOLS.—Additional symbols used in the construction of flow charts are as follows:

CONNECTOR SYMBOL. Represents a junction in a line of flow to another part of the flow chart. The entries and exits are represented by a set of two connector symbols. When flow charts are broken because of page limitations, this symbol is used to indicate the break, and identifications should be placed within the symbol.

rupt).

The following graphic symbols are used on flow charts and other documentation when appropriate:

+	plus, add
−	minus, subtract
*	multiply
/	divide
±	plus or minus
=	equal to
>	greater than
<	less than
≥	greater than or equal to
≤	less than or equal to
≠	not equal to
≯	not greater than
≮	not less than
YES or Y	Yes
NO or N	No
TRUE or T	True
FALSE or F	False

The general outline mentioned previously for calculating resistance values will now be diagrammed (flow charted). Certain additional parameters will be used to fully illustrate the preparation and use of flow diagrams. We will restate the original problem as follows: It is desired to determine the resistance of various circuits, each containing up to ten resistors in

code.

The program may be used as a subroutine if desired. If used as a subroutine, the value found for R_t is stored and an exit made from the subroutine. If not used as a subroutine, R_t is typed on the teletype and the R_t for the next circuit, if any, computed. This process continues until all circuits have been computed and typed.

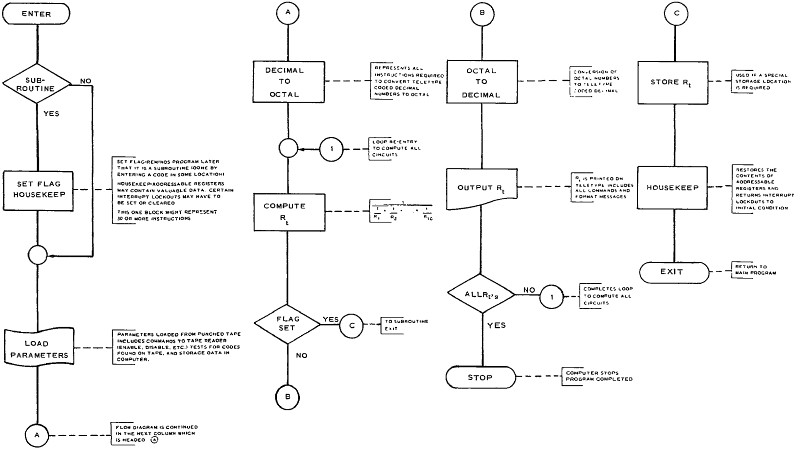
It is also assumed that if the program is used as a subroutine, the programmer does not know the contents of the various resistors.

The flow chart, taking these points into consideration, is shown in figure 1-52. A careful study of this figure brings several interesting facts to light. An important observation here is that the actual computation comprises a relatively small portion of the instructions. The total number of instructions could be reduced by performing the octal-to-decimal conversions outside the computer and by making the parameter entries directly on the entry panels of the computer and reading the solutions from it. These steps would negate the advantages of the computer, particularly on circuits that require a great many entries. An important fact to remember is that unless a relatively simple operation is to be performed a large number of times, there is no reason to program it.

MAINTENANCE PROGRAMS

As we have previously stated, a routine or program is a series of instructions that control the operations of a computer. Each instruction is used to cause some action which is part of the overall task that the computer must perform. Therefore, an instruction may be considered as the basic building block of a computer program.

An overall check of a computer can be done by the use of a maintenance program. The maintenance program provides a thorough and rapid method for the detection of failures in a specific portion of a computer. This type of overall maintenance check is flexible and efficient. The programs may use the same type tape, memory, computing and external storage media as operational programs. The maintenance program can be altered when the computer or


ENTER
SUB-ROUTINE
NO
YES
SET FLAG HOUSEKEEP
SET FLAG-REMINDS PROGRAM LATER THAT IT IS A SUBROUTINE (DONE BY ENTERING A CODE IN SOME LOCATION)
HOUSEKEEP-ADDRESSABLE REGISTERS MAY CONTAIN VALUABLE DATA. CERTAIN INTERRUPT LOCKOUTS MAY HAVE TO BE SET OR CLEARED
THIS ONE BLOCK MIGHT REPRESENT 30 OR MORE INSTRUCTIONS
LOAD PARAMETERS
PARAMETERS LOADED FROM PUNCHED TAPE INCLUDES COMMANDS TO TAPE READER (ENABLE, DISABLE, ETC.) TESTS FOR CODES FOUND ON TAPE, AND STORAGE DATA IN COMPUTER.
A
FLOW DIAGRAM IS CONTINUED IN THE NEXT COLUMN WHICH IS HEADED Ⓐ
A
DECIMAL TO OCTAL
REPRESENTS ALL INSTRUCTIONS REQUIRED TO CONVERT TELETYPE CODED DECIMAL NUMBERS TO OCTAL
1
LOOP RE-ENTRY TO COMPUTE ALL CIRCUITS
COMPUTE R_t
$\frac{1}{\frac{1}{R_1}+\frac{1}{R_2}+\cdots+\frac{1}{R_{10}}}$
FLAG SET
YES
C
TO SUBROUTINE EXIT
NO
B
B
OCTAL TO DECIMAL
CONVERSION OF OCTAL NUMBERS TO TELETYPE CODED DECIMAL
OUTPUT R_t
R_t IS PRINTED ON TELETYPE INCLUDES ALL COMMANDS AND FORMAT MESSAGES
ALLR_t's
NO
1
COMPLETES LOOP TO COMPUTE ALL CIRCUITS
YES
STOP
COMPUTER STOPS PROGRAM COMPLETED
C
STORE R_t
USED IF A SPECIAL STORAGE LOCATION IS REQUIRED
HOUSEKEEP
RESTORES THE CONTENTS OF ADDRESSABLE REGISTERS AND RETURNS INTERRUPT LOCKOUTS TO INITIAL CONDITION
EXIT
RETURN TO MAIN PROGRAM

164.136

Figure 1-52.—Parallel resistance computations flow diagram.

Testing by means of maintenance programs results in the computer circuits being used in a more comprehensive manner than during normal program execution. When a program has been checked and accepted as a good maintenance tool, it is not subject to deterioration. In contrast, test equipment may be checked and accepted only to become unreliable shortly after being placed in use.

Maintenance programs are divided into three main classes: reliability, diagnostic, and utility programs. Maintenance programs that are used to detect the existence of errors are called reliability programs. Reliability programs should be arranged to check as many computer circuits as possible.

Maintenance programs that are used to locate the circuits in which computer malfunctions originate are called diagnostic programs. An effective diagnostic program should locate the source of trouble as closely as possible. Actually, in many cases reliability programs have diagnostic features, and diagnostic programs have reliability features. For convenience, a program is called either a reliability or diagnostic program, depending on its intended emphasis. In general, programs that check rather than diagnose are shorter and simpler.

A utility program is a routine used in general support of a computer; for example, input/output tracing or monitoring routine. This term is used synonymously with service routines.

Program Instructions

An efficient program makes full use of the instructions to accomplish the task in the shortest possible time while the minimum number of instructions are used. In most cases, either time or the number of instructions has to be selected as the primary criterion when a program is developed. If time is important, the program should use instructions of short duration; however, it may use several memory locations for storage. If time is relatively unimportant, but only a few memory locations are available, instructions that do a number of things or cause the program to execute more than once should be used.

of the instruction, when the instruction may used, and the state of the computer after instruction has been carried out. In addition should be known whether the instruction can indexed and what internal conditions must satisfied before it can be executed.

HALT INSTRUCTION.—The halt instr tion causes the computer to stop execut instructions under program control. Howev any operation that is in progress at the time halt instruction is decoded will be comple first. For example, if information is being r into the memory from a deck of punched car all the cards will be read before the compu halts, even if the halt instruction was issued j after the reading operation began. The addr portion of the halt instruction is not us therefore, indexing is not possible. When computer is halted by instruction, the progr counter retains the address of the instruct immediately following, so that restarting computer will cause this next instruction to executed.

CLEAR-AND-ADD INSTRUCTION.— clear-and-add instruction is used to ente quantity into the accumulators from the mem section without changing the sign or magnit of the words. This instruction is normally u when it is desired to begin a type of addit problem. The accumulators are first clear and then the information selected from memory section by the address portion of clear and add instruction is transferred to computer registers. Addition of the data in registers and the data in the accumulator started; however, since the accumulators cleared to +0, this addition has the ove effect of transferring the word from the mem section into the accumulators unchanged. memory area used is unchanged, and the regis are cleared to +0 after execution of clear-and-add instruction.

ADD INSTRUCTION.—This instructio similar to the clear and add instruction exc that it does not provide for clearing accumulators before the addition process beg

This sum is placed in the accumulators, and the registers are cleared to + 0. You should be aware that the add instruction can cause an overflow if the numbers added together are sufficiently large. If this happens, the result in the accumulator is meaningless.

FULL-STORE INSTRUCTION.—The full-store instruction is used to transfer words from the accumulators into the memory area specified by the address portion of the instruction. Thus, the results of any operation performed by the arithmetic section are placed in the memory section for future use. The contents of the specified register are first cleared, and then the contents of the accumulators are transferred to the memory-section buffers.

Reliability Programs

Reliability programs are used in both preventive and corrective maintenance tests to detect circuit failures rapidly. Reliability programs are also used to discover failures that may occur only under particular operating conditions. Examples of troubles that are not evident at all times are failures that appear at specific repetition rates or for certain combinations of bits. To detect such failures, it is necessary to use reliability programs which check logical operation, paths of information flow, timing, ability of the computer to perform all functions, execution of instructions, and so on.

Reliability programs check either the logical functioning of an entire computer section or the logical functioning of individual circuit groups in a section. Whichever method is used, it is assumed that associated circuits which are not directly checked by the program are in satisfactory operating condition. Thus, these programs fall into two categories—first order and second order. First-order reliability programs check the operation of an entire computer section, while second-order programs check the operation of assemblies or circuit groups, such as registers, counters, and so forth. In most cases, first-order programs are merely a combination of several second-order programs.

A reliability program provides a good-or-bad indication regarding the ability of the tested time of relays within a specific section of a computer. As long as the switching time of the relays is within normal limits, the reliability program will indicate satisfactory operation. When the switching time is excessive, however, this means that maintenance is required. If the program is running successfully, there will be no failures within the checked area. In the event of a failure indication, the failure may be in the area being checked or in another area that has been assumed free of trouble. Diagnostic maintenance programs should then be used to locate the source of trouble.

Diagnostic Programs

To be efficient, maintenance programs for diagnostic applications must enable you to narrow the area of a failure down to the smallest possible number of circuits. This can be accomplished by using increasing-area, decreasing-area, overlapping-area, and large-area checks. The most effective method will depend on the particular type of computer being tested.

INCREASING-AREA CHECK.—A maintenance program using the increasing-area check initially tests a small number of circuits. If a check indicates that all tested circuits are operating properly, successive checks are run in which progressively greater numbers of circuits are added. By this method, circuits which are found to be operating correctly are used to check other circuits. This process is continued until all circuits that can be checked by a maintenance program have been tested.

DECREASING-AREA CHECK.—When this method is used to find a trouble, a large number of circuits are initially checked by the maintenance program. If trouble is detected in a large area, additional checks are made of successively smaller portions of the equipment until the stages affected by the failure are not included in the test area. You should then be able to determine which stages are defective. If the check of a large area reveals no error, the remaining large areas of the equipment are checked until the trouble is detected. In many cases, trouble can be located more rapidly by this procedure than by the increasing-area method.

area check. The routines of this type of maintenance program overlap each other. Thus, a failure is located at the overlapping portions of the routines which indicate the presence of trouble.

LARGE-AREA CHECK.—You may not be able to program an effective maintenance test for some small sections of a computer. A maintenance program can then be used only to detect the general area in which the malfunction occurs. When the general area is located, conventional trouble shooting is necessary to find the circuit in which a failure has occurred.

Utility Programs

Utility programs are used as aids for both operation and maintenance programming procedures. This type of program is used to print out information from magnetic cores, magnetic drums, or other storage devices within the computer memory section. It is also used to transfer maintenance programs from punched cards or magnetic tape into the computer memory section. Utility tracing programs provide a printed record of the contents of various computer registers to enable you to follow maintenance program operations.

MARGINAL CHECKING.—Marginal checking is a preventive-maintenance technique that is used for some Navy and commercial computer equipment to detect the decrease in reliability of circuit parts because of aging. Aging circuit parts almost invariably change in value, current-handling capabilities, or voltage limitations. Generally, the changes brought about by aging are gradual, and you will not notice any variation in the normal operation of the equipment. For maximum equipment reliability, parts that are beginning to deteriorate must be detected and replaced before a failure occurs.

operations of additions, subtraction, and so forth, while the program varies certain circuit parameters about their normal values. In this way, the computer is made to perform normal functions under controlled adverse operating conditions.

The amount of variation, from the normal value, that can be introduced before equipment failure occurs is called the margin of reliability of the circuit or group of circuits being tested. If the margin is regularly checked and its gradual decrease recorded; the time of circuit failure can be anticipated.

SUMMARY

In this section you have examined the evolution of the computer. In viewing this evolution and evaluating the consequences, you should bear in mind that the technologies involved with computers are advancing at a rapid rate. Even as you read this page what is presently considered state-of-the-art computer technology is rapidly becoming obsolete. In order to comprehend the new technologies, you will need to have an insight into what has already been accomplished.

A general description of various types of computers in use at the time of publication, along with a block diagram presentation of a typical computer, were presented in order to familiarize you with the construction of these units. An overview of the electronics circuits involved in a typical computer was also presented. It is very important that you comprehend the theory as set forth in this section. The following sections of this Rate Training Manual presupposes this background knowledge. You will also find this knowledge invaluable in answering the various items in the accompanying nonresident career course.

PART 2

IUSS COMPUTERS AND PROCESSORS

n this module part we will discuss the AN/ -20 computer, the Synchronous Distributed essor (SDP), and the AN/UYK-7 computer. se units have been selected for discussion use they are fairly typical of the computers processors used throughout the Ocean Sys- community. These computers and processors used for data analysis, communications, n forming, and display control. Upon the pletion of this module, you will be able to tify the AN/UYK-20 computer, the SDP, the AN/UYK-7 computer. You will also be to describe the physical makeup of these s and understand their basic operating ciples. An introduction to programming epts involving the AN/UYK-20 computer is ented to acquaint you with the operation of machine. From time to time you may find ecessary to refer to the glossary of terms ented in this module. You may also find it ful to review the theories presented in part you study certain sections of this module .

AN/UYK-20 COMPUTER

The AN/UYK-20 (figures 2-1 and 2-2) is a eral-purpose minicomputer used extensively ughout the Ocean Systems community. The /UYK-20 represents only one type of com- er used by the Ocean Systems community. vever, the theories and practices that apply he AN/UYK-20 can also be applied to other es of data processing sets (DPS). Therefore, following discussion applies to the AN/ K-20.

RPOSE AND CAPABILITIES

The AN/UYK-20 meets the various processing uirements of shore, shipboard, and sub- ine combat systems. It is used in applications requiring a small- to medium-scale data processing capability. The DPS shown in figure 2-3 is a modular, medium-scale, general-purpose digital data processing device that uses a microprogram control structure. (Microprogram concepts were discussed in the digital computer elements section of this module.) The microprogram consists of microinstructions and control data stored in read-only memory (ROM). The DPS operates from a stored program of macroinstructions read from main memory. The set can perform arithmetic operations, solve real-time problems, control other devices, and perform a wide variety of data processing functions. Some of these functions are described as follows:

- Performs one's and two's compliment integer arithmetic using signed numbers. The basic word length is 16 bits, which may be handled as 4-bit literals, 8-bit bytes (pronounced "bites") (such as ASCII character codes), 16-bit words, or as double-length 32-bit words.

- Has a memory-addressing capability of up to 65K 16-bit words, which may be treated as groups of pages (1K per page). The memory cycle time is 750 nanoseconds (nsec).

- Communicates with peripheral equipment through an input/output (I/O) controller containing up to 16 channels, which may be parallel or serial or a mixture of both.

- Has an interrupt structure, depending on priority assignments, which permits interruption of the normal program sequence to perform special functions.

- Allocates a portion of micromemory for a user-defined microprogram and diagnostic routine.

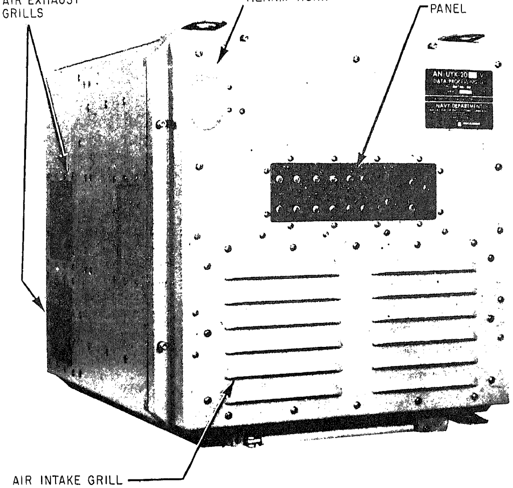


Figure 2-1.—Data Processing Set AN/UYK-20(V), front view.

- Has a real-time clock and monitor clock that operate either from an internal oscillator or from an external clock input.

- A mathpack option adds square root, floating point, trigonometric, hyperbolic, and double-precision multiply and divide capability.

COMPUTER COMPOSITION

Two different designators can be applied to the DPS. AN/UYK-20(V) applies to units configured for 400-Hz power. AN/UYK-20X(V) applies to units configured for 60-Hz power. The majority of units within the Ocean Systems community are configured for 60-Hz power. Throughout this section we will use the generic designator "AN/UYK-20" when referring to this computer. We will also point out any peculiarities that apply to a particular configuration.

The AN/UYK-20 consists of a single cabinet. A hinged door, called the control monitor, forms the front of the cabinet. Mounted on the frontside of this door is the operator's control panel (figure 2-1). This panel contains the basic controls and indicators used in the routine

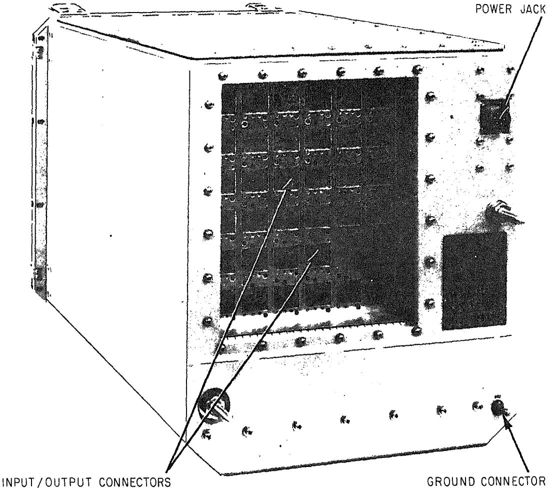


Figure 2-2.—Data Processing Set AN/UYK-20(V), rear view.

operation of the DPS. A more complete maintenance panel is mounted on the backside of the hinged door and is accessible only when the door is open. The air intake grill, filter, and alarm horn are also mounted on this door. Immediately behind the hinged door is the memory chassis (figure 2-4), which is hinged and mounted on slides. This design permits the chassis to be extended and completely exposed for servicing. Behind the memory chassis are the processor/IOC (input/output controller) chassis and the power supply. The rear panel of the cabinet (figure 2-2) contains the power jack and grounding stud and an opening for the I/O connectors, which are mounted on the backside of the processor/IOC chassis. The cooling fans of the CPU and power supply expell air through two air exhaust grills on the left side of the cabinet.

Processor/IOC

The processor/IOC chassis is commonly called the processor-verifier unit. It contains two sizes of printed circuit cards: single and triple width. The processor circuits are contained on single-width cards (figure 2-5), and the I/O circuits are contained on triple-width cards (figure 2-6). The guide pin connectors on newer AN/UYK-20 triple-width cards may vary from that shown in the figure.

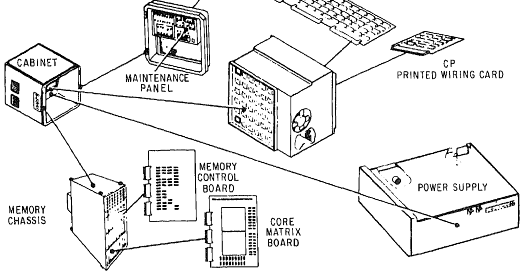


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Figure 2-3.—AN/UYK-20 modular architecture.

The single-width cards may be single or multilayered boards (as viewed from the edge), whereas the triple-width cards are contained on three layered boards. Single-width cards have one 56-pin interfacing connector. Triple-width cards have two multiple interfacing connectors, the position of which varies. Guide pins on the connectors are keyed to keep the cards from being inserted into the wrong jack. The shape of the cards keeps them from being inserted backwards into their jacks. In order to aid troubleshooting procedures, the cards contain test points along their top edges. A square blivet (figure 2-5) identifies the first test point (TP1). TP1 may be further identified by the rightmost test point when the card is mounted in the chassis. The last four digits of the card part number are color coded on the outer edge (as viewed from the front edge on) of each printed circuit card for ease of identification.

The rear panel of the processor/IOC chassis contains the I/O connectors. With the processor/IOC chassis removed from the cabinet, this panel can be removed for access to the I/O connector wire wrap points and the card connector wire wrap points (figure 2-7). The I/O connectors are keyed so input cables cannot be interchanged with output cables. The processor/IOC chassis is variable in that it contains a program kit, which varies according to the math pack and user-specified microprogram growth options. Another kit is available for 16 or 32 general registers. Various interface kits are also available, depending on the I/O types and interface levels required. Each kit consists of a specific set of circuit cards.

Memory

The memory is made up of three different types of circuit boards. These are Memory Control Board (MCB) (figure 2-8), Memory Data Board (MDB) (figure 2-9), and the core memory unit which is generally called the Memory Array Board (MAB) (figures 2-10 and 2-11). Actual board locations are shown in figure 2-4.

The MCB and MDB have keyed guide pins to prevent insertion in the wrong location. Each MCB contains control and addressing circuits for up to 32K of memory. Each MDB contains a data register and bit drivers for serving up to 32K of memory.

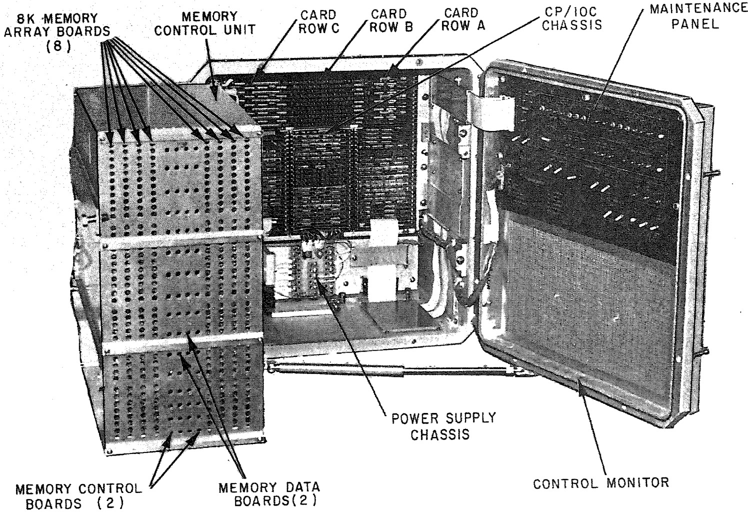

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Figure 2-4.—Data Processing Set AN/UYK-20 (opened out).

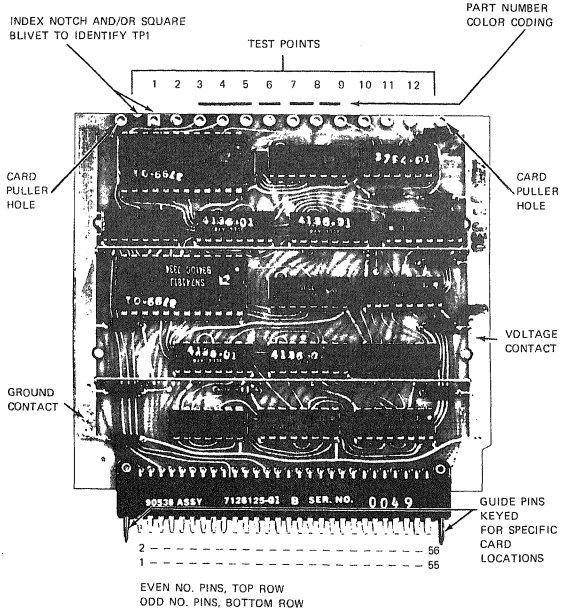

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Figure 2-5.—Typical single-width circuit card.

Each MAB contains an 8K × 16 bit core matrix, with associated drivers and sense amplifiers. The memory chassis contains two MCBs and two MABs and is called the core memory-control unit. From one to eight core-memory units (MABs) are inserted into the chassis to produce the required memory capacity, which can range from 8K to 65K 16-bit words. The majority of AN/UYK-20 units within the Ocean Systems community are configured for 8-memory array boards. Optional MCBs and MDBs have additional circuitry for a direct memory access (DMA) feature and may be specified as an option by the user.

The power supply (figures 2-12 and 2-13) is composed of a single chassis. In the event of a

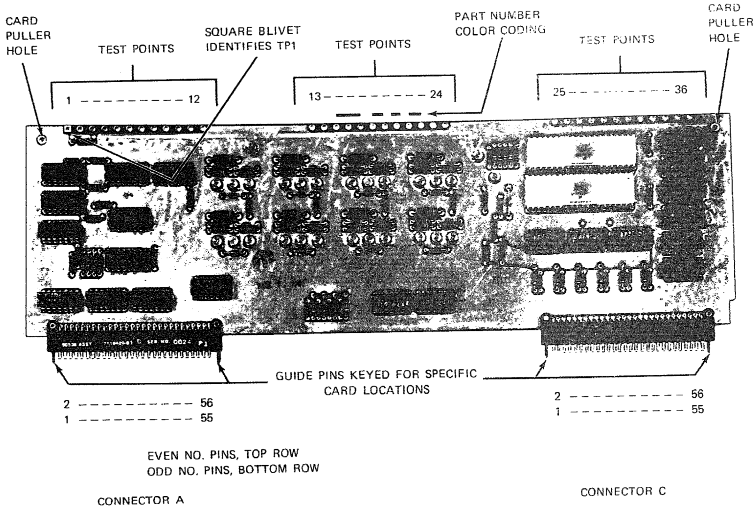

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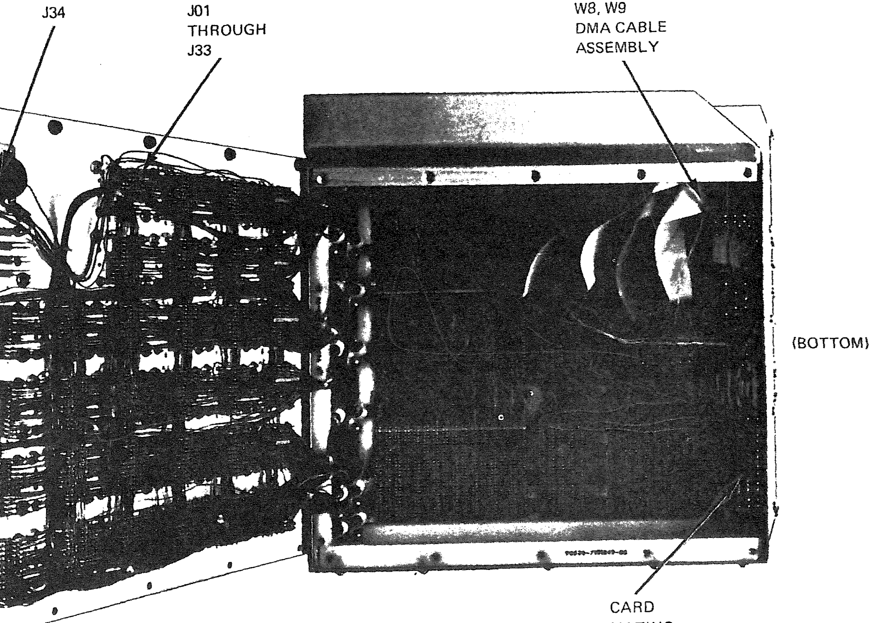
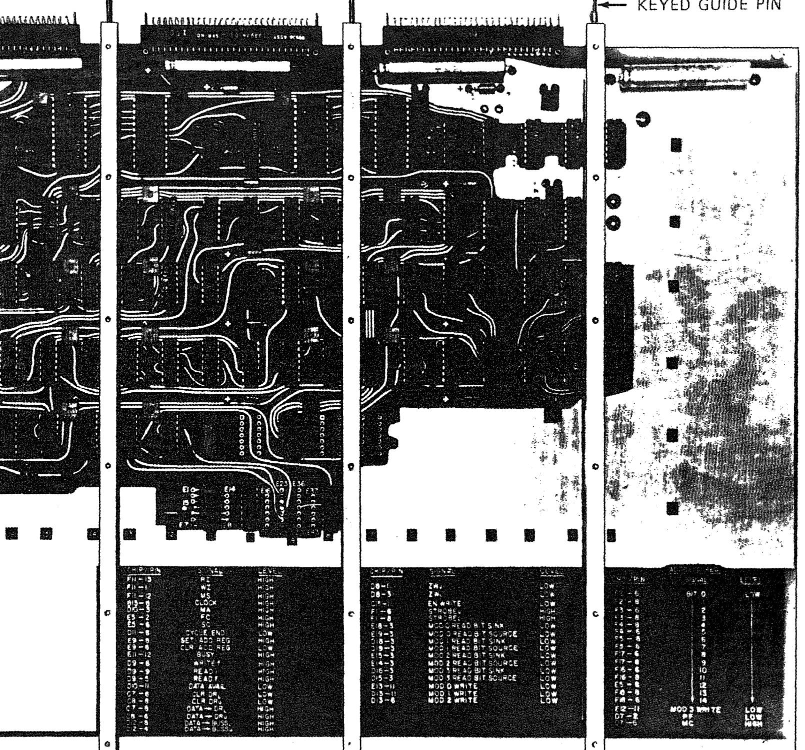
Figure 2-6.—Typical triple-width circuit card.

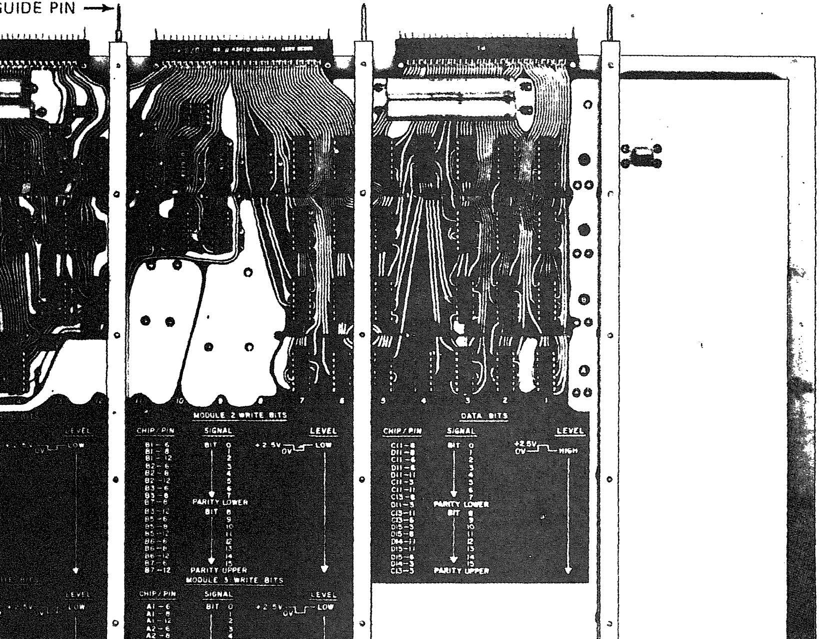

J34
J01
THROUGH
J33
W8, W9
DMA CABLE
ASSEMBLY
(BOTTOM)
CARD

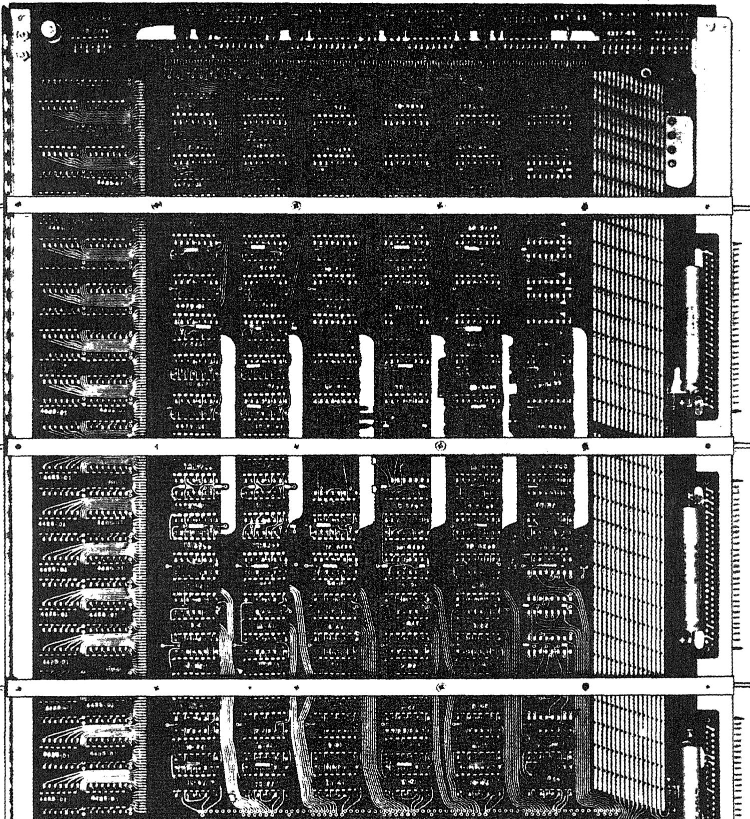


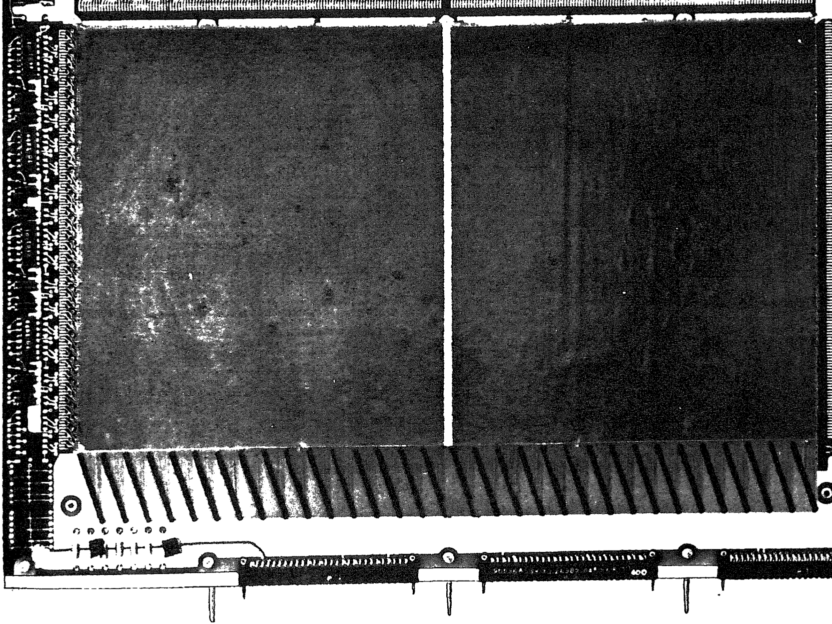
CHIP/PIN	SIGNAL	LEVEL
F11-13	RI	HIGH
F11-1	WI	HIGH
F11-12	MS	HIGH
B13-8	CLOCK	HIGH
D10-5	MA	HIGH
E3-2	FC	HIGH
E3-6	SC	HIGH
D11-8	CYCLE END	LOW
E9-8	SET ADD REG	HIGH
E9-6	CLR ADD REG	LOW
E11-12	BUSY	HIGH
D9-6	WRITE↑	HIGH
D9-9	READ↑	HIGH
D9-5	READ↑	HIGH
D10-11	DATA AVAIL	LOW
C7-6	CLR DR$_L$	LOW
C8-6	CLR DR$_U$	LOW
C7-8	DATA → DR$_L$	HIGH
C8-8	DATA → DR$_U$	HIGH
D12-8	DATA → BUSS$_L$	HIGH
D12-4	DATA → BUSS$_U$	HIGH

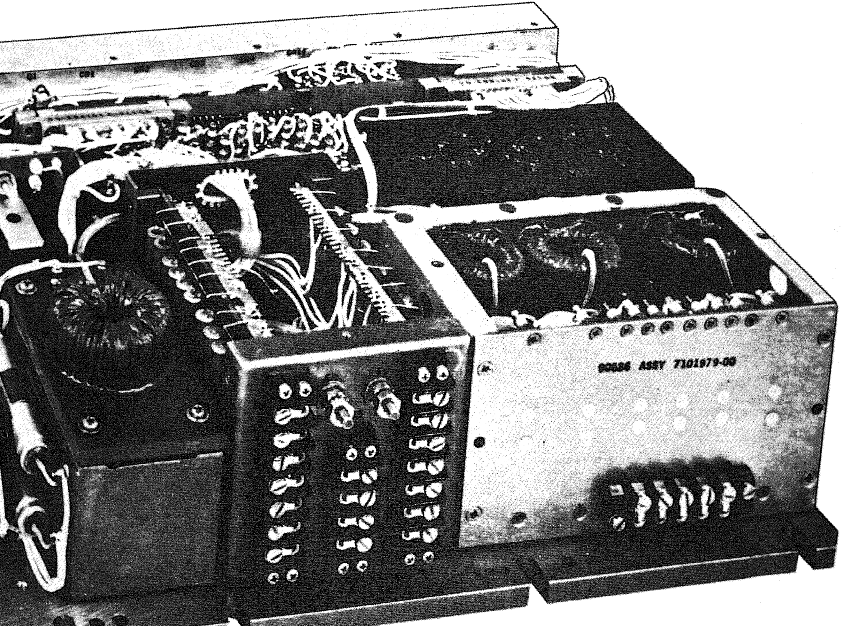
CHIP/PIN	SIGNAL	LEVEL
D8-1	ZW$_U$	LOW
D8-3	ZW$_L$	LOW
[illegible]	EN WRITE	LOW
F1-6	STROBE$_U$	HIGH
F1-8	STROBE$_L$	HIGH
E18-3	MOD 0 READ BIT SINK	LOW
E19-3	MOD 0 READ BIT SOURCE	LOW
D18-3	MOD 1 READ BIT SINK	LOW
D19-3	MOD 1 READ BIT SOURCE	LOW
E15-3	MOD 2 READ BIT SINK	LOW
E14-3	MOD 2 READ BIT SOURCE	LOW
D16-3	MOD 3 READ BIT SINK	LOW
D15-3	MOD 3 READ BIT SOURCE	LOW
E13-11	MOD 0 WRITE	LOW
D13-11	MOD 1 WRITE	LOW
D13-6	MOD 2 WRITE	LOW

CHIP/PIN	SIGNAL	LEVEL
F2-6	BIT 0	LOW
F2-8		
F3-6	2	
F3-8	3	
F4-8	4	
F4-6	5	
F5-8	6	
F5-6	7	
F7-6	8	
F7-8	9	
F6-6	10	
F6-8	11	
E5-8	12	
F8-8	13	
F8-6	14	
E12-11	MOD 3 WRITE	LOW
D7-2	PF	LOW
D7-6	MC	HIGH


GUIDE PIN
MODULE 2 WRITE BITS
CHIP/PIN
SIGNAL
LEVEL
B1-6 B1-8 B1-12 B2-6 B2-6 B2-12 B3-6 B3-8 B7-6 B3-12 B5-6 B5-8 B5-12 B6-6 B6-8 B6-12 B7-6 B7-12
BIT 0 1 2 3 4 5 6 7
PARITY LOWER
BIT 8 9 10 11 12 13 14 15
PARITY UPPER
+2.5V
0V
LOW
MODULE 3 WRITE BITS
CHIP/PIN
SIGNAL
LEVEL
A1-6 A1-8 A1-12 A2-6 A2-6
BIT 0 1 2 3 4
+2.5V
0V
LOW
DATA BITS
CHIP/PIN
SIGNAL
LEVEL
C11-8 D11-8 C11-6 D11-6 D11-11 C11-3 C11-11 C13-8 D11-3 C13-11 C13-6 D15-3 D15-8 D14-11 D15-11 D15-6 D14-3 C13-3
BIT 0 1 2 3 4 5 6 7
PARITY LOWER
BIT 8 9 10 11 12 13 14 15
PARITY UPPER
+2.5V
0V
HIGH
1
2
3
4
5
6
7
8
9
10
11






90536 ASSY 7101979-00

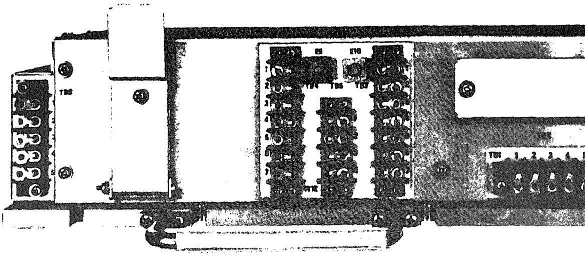


Figure 2-13.—Typical power supply, front view.

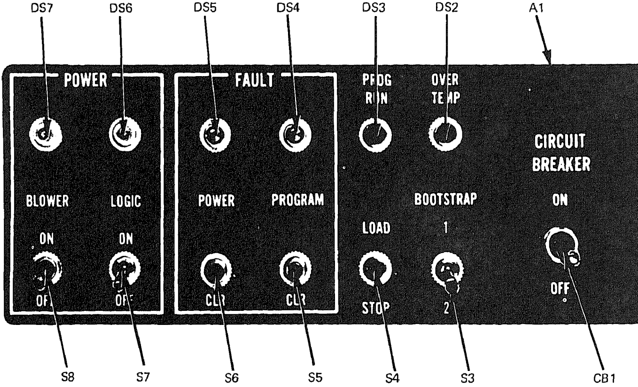
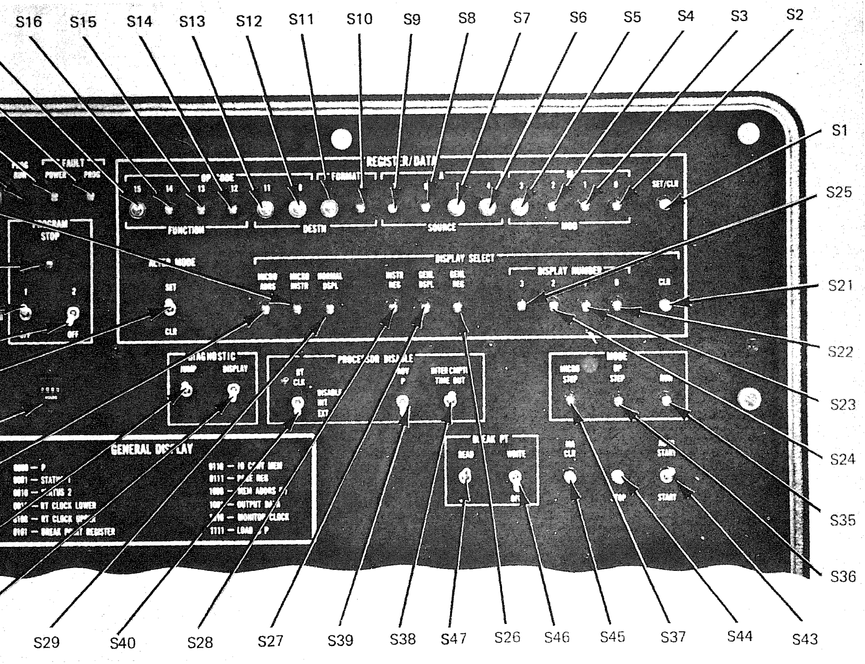


Figure 2-14.—Typical control panel.

power supply failure, you should process the power supply unit for turn-in rather than attempt-

stopping operations, operat
master clearing (master rese


S16
S15
S14
S13
S12
S11
S10
S9
S8
S7
S6
S5
S4
S3
S2
S1
S25
S21
S22
S23
S24
S35
S36
S29
S40
S28
S27
S39
S38
S47
S26
S46
S45
S37
S44
S43
REGISTER/DATA
FAULT
POWER
PROG
OP CODE
FORMAT
A
SET/CLR
FUNCTION
DESTN
SOURCE
MOD
PROGRAM
STOP
ALTER MODE
SET
CLR
OFF
OFF
DISPLAY SELECT
MICRO ADRS
MICRO INSTR
NORMAL DSPL
INSTR REG
GENL DSPL
GENL REG
DISPLAY NUMBER
CLR
DIAGNOSTIC
JUMP
DISPLAY
PROCESSOR DISABLE
RT CLK
DISABLE INT EXT
INTERCMPTR TIME OUT
MODE
MICRO STEP
OP STEP
RUN
BREAK PT
READ
WRITE
STOP
START
GENERAL DISPLAY
0000 — P
0001 — STATUS 1
0010 — STATUS 2
0011 — RT CLOCK LOWER
0100 — RT CLOCK UPPER
0101 — BREAK POINT REGISTER
0110 — IO CONT MEM
0111 — PAGE REG
1000 — MEM ADRS
1001 — OUTPUT DATA
1110 — MONITOR CLOCK
1111 — LOAD P

182 100-13

cators is located on the inside of the front door. This panel provides an effective aid to general servicing and program manipulation. The functions of the indicators and switches of the operator control and maintenance panels are illustrated in tables 2-1 and 2-2.

PROGRAMMING CONCEPTS

The functions that a computer can perform are ultimately determined by the array of instructions (commonly referred to as a repertoire), which allow it to function. The repertoire of the AN/UYK-20 encompasses nearly 200 executable instructions. These instructions, by themselves, can be changed to provide several variations of each instruction.

Instruction Words

Instruction words "tell" the computer what function it is to perform. (We will describe an instruction word shortly.) An instruction word may also tell the computer to combine two particular items (data words). When combined in a logical fashion, a group of these instruction words form a program. (A program is defined as a group of instructions that perform a complex function.) Individual instruction words perform relatively simple tasks. By performing a large number of simple tasks in an orderly manner, the computer can perform complex tasks.

Programs are constructed by placing several instructions in consecutive memory locations. A register called the "P" register keeps track of the next instruction to be executed. For example, the following program may be located in memory:

Memory Location	Instruction Words
P = 001000	Instruction #A
001001	Instruction #B
001002	Instruction #C

When the computer begins to execute this

of these formats, we w
of a typical add instr
formats. It must be st
add instruction is repre
of instruction, which t
of executing.

Add Instruction Desc

An add instruction
the following discuss
tells the computer to
place the sum into a
central processor (C
must be able to tell th

- To perform an
- Where to place
- Where to obtai
- Where to obtai

62
+ 40
102

In all add instructi
from a particular set (
whichever register cor
receive the sum of t
selected determines wh

RR FORMAT.—
means register to reg
from the same set of r
augend for the additi
simply means a num
added to a number i
reference is used in R

RI FORMAT.—
immediate (main) me
associated with jum
forms operations usin
memory as references

Table 2-1.—Control panel switches and indicators

IDENTIFICATION	TYPE	FUNCTION
CIRCUIT BREAKER ON/OFF (CB1)	Two-position toggle switch	ON position enables primary power to the DPS. OFF position disables primary power to the DPS.
BLOWER POWER ON/OFF (S8)	Two-position toggle switch	ON position enables power to the DPS cooling fans and enables LOGIC POWER ON/OFF switch function. OFF position disables power to the DPS cooling fans and disables LOGIC POWER ON/OFF switch function.
BLOWER POWER (DS7)	Indicator (neon with white lens)	When lit, indicates blower power is applied.
LOGIC POWER ON/OFF (S7)	Two-position toggle switch	ON position enables power to the dc power supply. OFF position disables power to the dc power supply.
LOGIC POWER (DS6)	Indicator (incandescent with white lens)	When lit, indicates dc power is applied.
POWER FAULT (DS5)	Indicator (red LED with clear lens)	When lit, indicates a Power Fault Interrupt has occurred (see paragraph 3-63).
POWER FAULT CLR (S6)	Two-position return-to-neutral toggle switch	When momentarily operated to the CLR position, clears the POWER FAULT indicators on both the control panel and the maintenance panel.
PROGRAM FAULT (DS4)	Indicator (red LED with clear lens)	When lit, indicates a CP or IOC Instruction Fault Interrupt has occurred, caused by attempting to

Table 2-1.—Control panel switches and indicators—Continue

IDENTIFICATION	TYPE	FUNCTION
PROGRAM FAULT CLR (S5)	Two-position return-to-neutral toggle switch	When momentarily operat CLR position, clears the P FAULT indicator on the c panel and the PROG FAU on the maintenance panel.
PROG RUN (DS3)	Indicator (green LED with green lens)	When lit, indicates DPS is instructions in Run mode.
OVER TEMP (DS2)	Indicator (neon with red lens)	When lit, indicates DPS in cabinet air temperature ha to 57°C, which is within 1 of the maximum temperat the DPS can operate safel power supply heat sink ha 76°C which is within 13° maximum temperature.
ALARM (LS1)	Audible	This alarm sounds if the A ENABLE/DISABLE/TES the ENABLE position and internal cabinet air tempe has risen to 57°C, which i within 13°C of the maxim temperature at which the operate without risking co damage, or the temperatu power supply heat sink ha 76°C which is within 13° the maximum temperatur
ALARM ENABLE/ DISABLE/TEST (S2)	Three-position toggle switch	ENABLE position enables alarm function. DISABLE position disable audible alarm function.

Table 2-1.—Control panel switches and indicators—Continued

IDENTIFICATION	TYPE	FUNCTION
BATTLE SHORT ON/OFF (S1)	Two-position toggle switch	ON position disables the over-temperature shutdown function. OFF position enables the over-temperature shutdown function.
BATTLE SHORT (DS1)	Indicator (neon with red lens)	When lit, indicates BATTLE SHORT switch is in the ON position.
BOOTSTRAP 1-2 (S3)	Two-position toggle switch	Selects one of two possible bootstrap programs in the NDRO memory. Operates in conjunction with the Op Code = 40 RR, a = 7 Conditional Jump macroinstruction and may be used, at programmer's discretion, to control branching in other programs.
LOAD/STOP (S4)	Three-position return-to-neutral toggle switch	When momentarily operated to the LOAD position, causes the DPS to execute a master clear, select Run mode, then begin executing instructions beginning from NDRO address 002. When momentarily operated to the STOP position, causes the DPS to stop executing instructions.

Table 2-2.—Maintenance panel switches and indicators

IDENTIFICATION	TYPE	FUNCTION
AUTO START/ START (S43)	Three-position toggle switch	When set to the AUTO STAR causes the DPS to begin execu instructions at NDRO bootst address 000 when power is ap is restored after a power failu When momentarily operated START position, causes the begin executing instructions mode selected.
STOP (S44)	Two-position return-to-neutral toggle switch	When operated to the STOP while the DPS is executing in tions in the Run mode, cause DPS to stop executing macro
MA CLR (S45)	Pushbutton switch	When operated while the DPS Run condition, the DPS reset master cleared state*. When operated while the DPS Run mode, clears the FAULT on the control and maintenan
BREAK PT READ/OFF (S47)	Two-position toggle	READ position causes the D executing instructions after r data from the memory addre by the contents of the break register. The instruction duri breakpoint occurred, includi related operand references, if will be completed before sto position disables the read sto
BREAK PT WRITE/OFF (S46)	Two-position toggle	WRITE position causes the D executing instructions after w data in the memory address s by the contents of the break register. OFF position disable

Table 2-2.—Maintenance panel switches and indicators—Continued

IDENTIFICATION	TYPE	FUNCTION
PROG RUN (S20)	Indicator-switch (green LED with green lens)	Indicator function: When lit, indicates the DPS is executing instructions in the Run mode. Switch function: Selects run condition in Micro Step mode.
POWER FAULT (S19)	Indicator-switch (red LED with clear lens)	Indicator function: When lit, indicates a Power Fault Interrupt has occurred (see paragraph 3-63). Switch function: When operated clears the POWER FAULT indicators on both the operator's control panel and the maintenance panel.
PROG FAULT (S18)	Indicator-switch (red LED with clear lens)	Indicator function: When lit, indicates a CP or IOC Instruction Fault Interrupt has occurred caused by attempting to execute an illegal instruction. Switch function: When operated, clears the PROGRAM FAULT indicator on the operator's control panel and the PROG FAULT indicator on the maintenance panel.
PROGRAM STOP (DS1)	Indicator (red LED with clear lens)	When lit, indicates a programmed stop has been executed.* (40 RR, RK, RX, A = 11, 12, or 13.)**
PROGRAM STOP 1/OFF (S34)	Two-position toggle switch	In 1 position, causes a program stop when the DPS executes a stop-jump macroinstruction (40 RR, RK, RX with an A-value = 12).**
PROGRAM STOP 2/OFF (S33)	Two-position toggle switch	In 2 position, causes a program stop when the DPS executes a stop-jump macroinstruction (40 RR, RK, RX with

Table 2-2.—Maintenance panel switches and indicators—Continued

IDENTIFICATION	TYPE	FUNCTION
Time meter (M1)	4 digit, 0000 to 9999	Records accumulated hours tha power has been applied.
DIAGNOSTIC JUMP (S42)	Two-position toggle switch	In the JUMP position, enables branching on the F = 14, M = Branch microinstruction. Its us causes the DPS to jump from t operating microprogram to the diagnostic microprogram when is master cleared. It is also used with the diagnostic return mac tion (00 RR) to provide a mea return to the diagnostic microp from the diagnostic macroprog Appendix A for a description o RR macroinstruction.) When used in connection with DSPL, GENL DSPL, DISPLAY and MICRO STEP it enables m loading of the micro P register. paragraph 2-21.)
DIAGNOSTIC DISPLAY (S41)	Two-position toggle switch	In the DISPLAY position while is in the Micro Step mode: a. With MICRO ADRS set, DATA displays the addres next microinstruction to b executed. b. With MICRO INSTR set, DATA displays the microi currently being executed. c. With NORMAL DSPL set, DATA displays the data o source bus as directed by microinstruction currently executed.

Table 2-2.—Maintenance panel switches and indicators—Continued

IDENTIFICATION	TYPE	FUNCTION
PROCESSOR DISABLE: RT CLK DISABLE/INT/EXT (S40)	Three-position toggle switch	DISABLE position inhibits incrementing of the Real-Time Clock register and the Monitor Clock register. INT position causes the Real-Time Clock register and the Monitor Clock register to use the internal clock source for timing. EXT position causes the Real-Time Clock register and the Monitor Clock register to use the external clock source for timing.
PROCESSOR DISABLE: ADV P (S39)	Two-position toggle switch	Up position inhibits incrementing of the P-register, thus causing the DPS to repeatedly perform one 16-bit macroinstruction. Will not properly execute RK and RX instruction.
PROCESSOR DISABLE: INTERCMPTR TIME OUT (S38)	Two-position toggle switch	Up position inhibits the occurrence of a Class III Intercomputer Timeout Interrupt.
MODE: MICRO STEP (S37)	Indicator-switch (red LED with clear lens)	Indicator function: When lit, indicates DPS is in Micro Step mode to execute a single microinstruction. (To clear, depress DISPLAY SELECT CLR switch.) Switch function: When operated, places DPS in Micro Step mode.
MODE: OP STEP (S36)	Indicator-switch (red LED with clear lens)	Indicator function: When lit, indicates DPS is in Op Step mode or in Micro Step mode to execute a single macroinstruction.

Table 2-2.—Maintenance panel switches and indicators—Continued

IDENTIFICATION	TYPE	FUNCTION
MODE: RUN (S35)	Indicator-switch (red LED with clear lens)	Indicator function: When lit, in cates DPS is in Run mode or in Step mode to execute successive tions. Switch function: When operate Op Step mode and enables the
DISPLAY SELECT CLR (S21)	Pushbutton switch	When operated, clears DISPLAY 0 through 3 and clears the Micr mode.
ALTER MODE SET/CLEAR (S32)	Two-position toggle switch	In the SET position (normal ope a. Causes individual bit of reg being displayed to set whe corresponding REGISTER indicator switch is operate b. Causes all bits of register being displayed to clear wh REGISTER/DATA SET/C operated. In the CLEAR position (altered a. Causes individual bit of reg being displayed to clear wh corresponding REGISTER cator switch is operated. b. Causes all bits of register b displayed to set when REG DATA SET/CLR switch is
REGISTER/DATA SET/CLR (S1)	Pushbutton switch	When operated, sets or clears all bits of register being displayed i REGISTER/DATA indicator sw through 15, dependent on ALT SET/CLEAR positio

Table 2-2.—Maintenance panel switches and indicators—Continued

IDENTIFICATION	TYPE	FUNCTION
REGISTER/DATA 0 through 15 (S2 – S17)	Indicator-switches (red LED with clear lens)	Indicator function: Display contents of selected register. Switch function: Modify contents of selected register depending on position of ALTER MODE switch.
DISPLAY SELECT: MICRO ADRS (S31) MICRO INSTR (S30) NORMAL DSPL (S29) INSTR REG (S28) GENL DSPL (S27) GENL REG (S26) DISPLAY NUMBER 3–0 (S22 – S25)	Indicator-switches (red LED with clear lens)	Indicator function: When lit as specified in table 2-3, indicates REGISTER/ DATA is displaying the corresponding register. Changing the contents of REGISTER/DATA changes the contents o the register being displayed. Switch function: When operated as specified in table 2-3, causes REGISTER DATA to display the corresponding register contents. Operation of any one of MICRO ADRS, MICRO INSTR, or NORMAL DSP causes the other two to clear. Operation of any one of INSTR REG, GENL DSPL, or GENL REG causes the other two to clear.

MICRO ADRS	MICRO INSTR	NORMAL DSPL	INSTR REG	GENL DSPL	GENL REG	DISPLAY NUMBER				REGISTER SELECT
						3	2	1	0	
1	0	0	X	X	X	X	X	X	X	μP Register (MICRO STEP and I DISPLAY selected) (Note 2) (No
0	1	0	X	X	X	X	X	X	X	μI Register (MICRO STEP and D DISPLAY selected) (Note 2)
0	0	1	X	X	X	X	X	X	X	Source Bus (MICRO STEP and D DISPLAY selected) (Note 2)
0	0	1	1	0	0	X	X	X	X	Instruction Register
0	0	1	0	1	0	0	0	0	0	P Register
0	0	1	0	1	0	0	0	0	1	Status Register 1
0	0	1	0	1	0	0	0	1	0	Status Register 2
0	0	1	0	1	0	0	0	1	1	RTC Register, Lower 16 Bits
0	0	1	0	1	0	0	1	0	0	RTC Register, Upper 16 Bits
0	0	1	0	1	0	0	1	0	1	Breakpoint Register
0	0	1	0	1	0	0	1	1	0	I/O Control Memory (Note 1)
0	0	1	0	1	0	0	1	1	1	Page Register (IR 5–0 selects re
0	0	1	0	1	0	1	0	0	0	Memory Address Contents (P sel
0	0	1	0	1	0	1	0	0	1	Output Data (IR A-field selects
0	0	1	0	1	0	1	0	1	0	Monitor CLock Register (Note 2
0	0	1	0	1	0	1	1	1	1	Load μP (Note 3)
0	0	1	0	0	1	0	0	0	0	General Register R0
0	0	1	0	0	1	0	0	0	1	General Register R1
0	0	1	0	0	1	0	0	1	0	General Register R2
0	0	1	0	0	1	0	0	1	1	General Register R3
0	0	1	0	0	1	0	1	0	0	General Register R4
0	0	1	0	0	1	0	1	0	1	General Register R5
0	0	1	0	0	1	0	1	1	0	General Register R6
0	0	1	0	0	1	0	1	1	1	General Register R7
0	0	1	0	0	1	1	0	0	0	General Register R10 (
0	0	1	0	0	1	1	0	0	1	General Register R11
0	0	1	0	0	1	1	0	1	0	General Register R12
0	0	1	0	0	1	1	0	1	1	General Register R13
0	0	1	0	0	1	1	1	0	0	General Register R14
0	0	1	0	0	1	1	1	0	1	General Register R15
0	0	1	0	0	1	1	1	1	0	General Register R16
0	0	1	0	0	1	1	1	1	1	General Register R17

ruction of a computer program, the pro-
mer is not concerned with the data values—
vhere the data is located.

K FORMAT.—In dealing with an addition
em, the addend is usually known (for
ple, X + 3). In this case, "3" is constant
when used in a program, is called a program
ant. The RK format (which means konstant-
gister) allows the instruction word to define
gram constant. Thus, operands (data words
iantities to be operated upon) can be in a
er, main memory, or defined in the program.
RK format is double-length (32-bit) and does
nake a memory reference.

L FORMAT.—The RL format means literal
gister. A literal is a special 4-bit word that
fined in the instruction word for the RL
at. RL formats perform operations such as
shifts (left or right) and specialized mathe-
cal operations for adding, subtracting, load-
multiplying, comparing, and dividing.

puter Registers

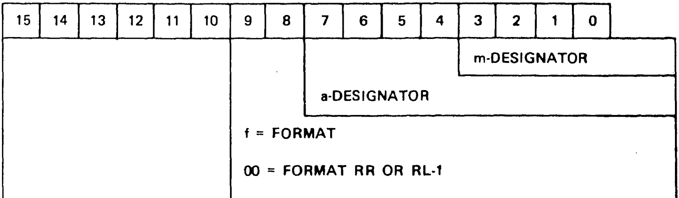
here are a number of registers in the CP
on of the AN/UYK-20. Those registers,
e contents can be changed by a program or
n instruction being executed, are called
essable and/or general registers. When an
nd is required for an add instruction, it
es from a particular set of registers called
operations is always placed in the general re
which makes these registers program addre
Other registers in the AN/UYK-20 th
program addressable include the following:
registers #1 and #2, the real-time clock (upp
lower), the "P" register, and the monitor

Registers that are not program addre
include those not directly referenced by
struction. Included in this category are th
and accumulator registers. The contents o
registers may change during instruction
tions. It is not, however, the purpose
program instructions to directly addres
change the contents of these registers. Th
say that the contents of the addressable re
may be altered by the program and these i
may influence the contents of the nonaddre
systems.

Format Analysis

Our previous discussion gave a general
review of the instruction word formats use
the AN/UYK-20. In the following paragra
will provide a more detailed analysis of th
RI, RK, RX, and RL formats. The RR, R
RL formats are 16 bits in length, while t
and RX formats are 32 bits in length.

INSTRUCTION WORDS.—Instru
words are written in a particular man
format. Figure 2-16 illustrates the most com



Instruction words use special fields or designators. Bit positions 15 to 10 in figure 2-16 compose a designator (field) called an operation code or simply an OP code. Every instruction in the AN/UYK-20 contains this OP code field. The six bit positions of the field can contain a value of 00-77_8. An OP code field is used to tell the computer what to do; for example, add, subtract, or load data into a register. Bit positions 9 and 8 designate the format of the instruction word. Bit positions 7 to 4 define the a-designator (general register number). Bit positions 3 to 0 define the m-field (general register number). We will present a more detailed discussion of instruction word formats later in this section.

ADDRESS WORDS.—As we discussed previously, it is not always necessary for a programmer to know exactly what a data word is (quantity, sign, and so forth). It is necessary, however, to know where a data word is located. The memory capacity of the UYK-20 is about 65K words. Each memory location is unique and is assigned a number called an address. In the AN/UYK-20, words may be encountered that are neither instruction nor data words, but are address words. Address words are kept in a register in the CP section of the computer and are sent to the memory section of the computer.

only address words. The "
the memory address of the
executed. The general regis
address words, which are
locate data.

DATA WORDS.—Th
four different data words.
data word is the 16-bit (
(see figure 2-17). Single-le
written as a two's complen
position 2^{15} containing t
position 2^{15} is a "0", th
number. A "1" in bit pos
negative number.

Single-length data wo
occupy a register or me
example, each general regis
so that the single-length w
bits, completely fills the reg
are also 16 bits in length.

Some instructions in t
specify a 32-bit data wo
32-bit word is called a dou
32-bit words may be locate
the general registers. Wher
the double-length word wil
locations (each memory l
length). For example, mem

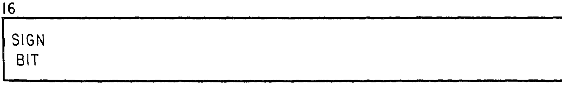
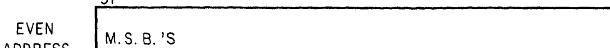


Figure 2-17.—Single-length data word.



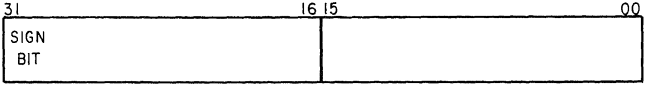
001003 could contain a 32-bit word. If a le-length word is in two consecutive memory ons, the most significant 16 bits are located e lower numbered address, and the lower ber address must be even. Figure 2-18 rates this situation.

he AN/UYK-20 treats the double-length much the same as a single-length word. The t word is a two's complement number with ign bit in bit position 2^{31}. Figure 2-19 rates the double-length word as it is handled e AN/UYK-20.

ouble-length words can also appear in the ection of the computer. The general registers he only registers that can contain a 32-bit . Two consecutive general registers must be o accommodate a 32-bit word. For example, nd R07 can contain a double-length word. is case, R06 contains the most significant and R07 contains the least significant

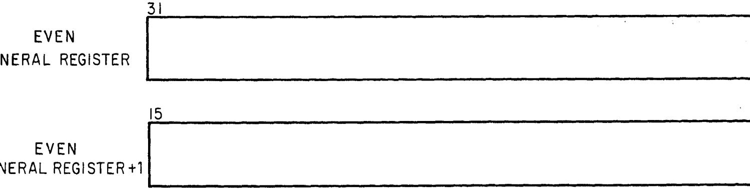
When two consecutive general register tain a double-length word, the most signi bits must be contained in the lower num general register, and the register number m even. For example, general registers R04 an can contain a double-length word. (The would be in R04, and R04 would be However, R11 and R12 cannot contain a word because the lower numbered general r (R11) is not even. Figure 2-20 shows a d length word in general registers.

Thus far, we have discussed the two ty data words used with the AN/UYK-20: the length and double-length words. A third t data word used with the AN/UYK-20 is the For the AN/UYK-20, a byte is an 8-bit Sign bits are not used with the byte and the are not referred to as positive or negative. a byte is loaded into a general register always loaded into the lower 8 bits. Figur illustrates this concept.



18

Figure 2-19.—Double-length word.



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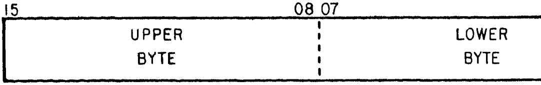


Figure 2-22.—Upper and lower byte (memory).

A byte, because it is only 8 bits in length, occupies one half of the bit positions of a general register or memory location. A byte in a memory location can occupy either the upper or lower half of the 16-bit field, whereas a byte in a general register always occupies the lower 8-bit positions. (See figure 2-22.)

When a byte is contained in a memory location it is called the upper byte or lower byte, depending on what bit positions it occupies.

Still another type of data word used with the AN/UYK-20 is the literal. A literal is a 4-bit number found in the general registers. A literal does not use a sign bit and occupies bit positions 00 to 03 of a general register. Literal numbers are defined by instruction words in the RL format.

Instruction Classifications

The function of the AN/UYK-20 is to execute programs. The programs, which are stored in memory, consist of small incremental steps called instructions. Instructions are grouped together in such a way that they result in the accomplishment of an orderly and sometimes quite complex task. Viewed individually, instructions are quiet simple in their execution.

Instructions that can be executed by the AN/UYK-20 are categorized into six basic groups:

- Data transfers

We will define the fun
the next paragraphs.

DATA TRANSFE
Simply stated, data t
used to move data
AN/UYK-20 to anoth
usually move data from
CP or vice versa. Data
register to register withi
are classified into two

- Loads—Data wi
to some register in the

- Stores—Data wi
to some location in ma

Loads and stores a
tions that can be group
There are no instructio
movement of data from
another.

Data transfer instru
gic placement of data

JUMP INSTRUCT
tions allow for the c
program. The followin
nature of a jump instru

or example, consider the following pro- portion:

Iemory ocation	Instruction Words	Memory Location	Instruction Words
01000	Instruction #A	004000	Instruction #X
01001	Instruction #B	004001	Instruction #Y
01002	Jump to 004000	004002	Instruction #Z

hus, in the preceding program portion, the uter would execute each instruction sequen- beginning with instruction 001000. Upon ompletion of instruction 001001, the "P" er would increment to 001002. At this the jump instruction causes the computer ump" to address 004000 and start sequential ction executions from this point.

onditional/Unconditional Jump Instruc- .—The concepts of conditional and uncon- nal are used to describe jumps. Unconditional es that an event will occur regardless of mstances. Unconditional jump instructions esult in a program jump each time they are ted.

onditional jump instructions on the other will result in a program jump only if a etermined condition has been satisfied. For ple, the instruction will tell the AN/UYK-20 ecute a jump only if a general register is not l to 0. In this case, a general register value than 0 will cause the jump instruction to ecuted. For values equal to 0, the computer gnore the jump and execute the next sequen- nstruction.

onditional jump instructions require the UYK-20 to make a decision. This may be l on the zero condition of a particular ter, the presence of a predetermined positive egative value, or the state of a flip flop.

RITHMETIC INSTRUCTIONS.—The tion of arithmetic instructions is very much

- Multiplication.
- Division.
- Trigonometric and hyperbolic fun
- Floating point formatted operatio

Arithmetic instructions are needed t form calculations required by the pro These instructions can be used to perform plex mathematical operations.

LOGIC AND SHIFT INSTRUCTIO The AN/UYK-20 can execute three ty logical instructions. These logical instru can be related to the AND, OR, and exc OR logic gate junctions. In this case, ever, the result is obtained by the com use of hardware and software. Shift in tions "shift" the contents of various re either right or left to facilitate data man tion.

I/O AND INTERRUPT CONTRO STRUCTIONS.—I/O and interrupt c instructions are used to control inform flow into or out of the AN/UYK-20. instructions also allow for the direct con interrupts that can be issued to or fro AN/UYK-20.

MISCELLANEOUS INSTRUCTIO Any instruction that cannot be categorize one of the preceding groups falls int category of instructions. Examples of falling into the miscellaneous categor instructions to count the number of "1" a general register or the "reverse register i tion," where the order of bits in a g register is reversed.

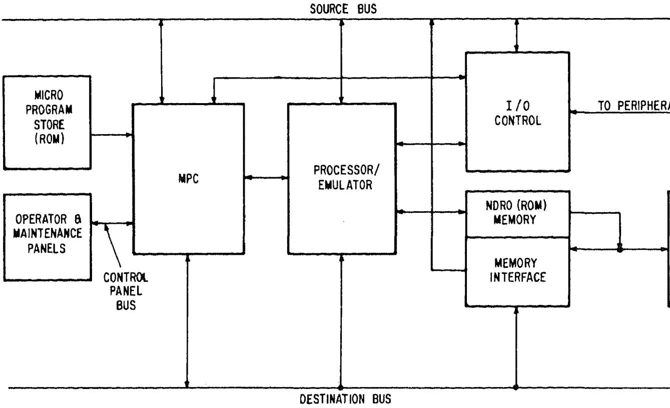


Figure 2-23.—Functional block diagram of the Data Processing Set AN/UYK-20(V)

FUNCTIONAL DESCRIPTION

The AN/UYK-20 is organized around a microprogram controller (MPC) and a two-bus data exchange structure (a 16-bit source bus and a 16-bit destination bus) (figure 2-23). The various functional elements accept bit configuration from the source bus, interpret and manipulate it, and, when appropriate, return bit-configured information to the destination bus for acceptance by another functional element. The destination bus provides an additional communication path between the arithmetic and logic units and the various registers, which allows the system to overlap functions. Control signals between sections do not use the busses, but are wired directly.

operations as directed by a prog
tions. The I/O circuits facilitat
between the computer and pe
ments. The main memory stor
operands, and other data. The
and memory interface circuits
trol of a microprogrammed co
operates from its own microp
in a ROM. The following is
the components of the DPS a
figure 2-24, a foldout located
part 2 of this module.

MICROPROGRAM CO
(MPC).—The MPC provides a
tions that enable the computer
program stored in main memory
and executes its own microprog

s. This set-up allows microinstruction apping since the MPC fetches the next ntial macroinstruction while still executing resent macroinstruction. This overlapping the effect of increasing the execution

ne MICRO MEMORY is a ROM capable olding up to 4K (4096) words of microam, including 512 addresses used for nal routines (as specified by the user). oprograms can be changed only by tuting different preprogrammed cards.

ne MICRO MEMORY CONTROL section ins the addressing circuits that control the ng of the MICRO MEMORY.

ne MICRO FUNCTION CONTROL sececeives the current microinstruction from RO MEMORY, translates it, then sends ol signals to all parts of the DPS to out the instruction. It includes the r clock that provides timing for the entire

ne REPEAT CONTROL section controls epetitive cycling of microprogram subnes as required by the repeat microinstruc-

ne ARITHMETIC/LOGIC section contains nulator storage registers and an Arithmetic Unit (ALU), which performs arithmetic ogic operations on the operands.

ne DISPLAY CONTROL section, under control of a microprogram subroutine, des the interface between the operator and tenance panels and the displayable registers e DPS.

ROCESSOR/EMULATOR.—The PRO-

The FUNCTION CONTROL section t lates the macroinstruction word and senc emulator control word (ECW) to the directing it to perform the microprogram ro for accomplishing each macroinstruction.

The general registers section can be use accumulator storage, for scratch pad regi for index registers, and so forth. The ge registers are normally addressed by the sp fields of the macroinstruction word. There be one or two groups of general registers (specified options within the Ocean Sys community specify two sets of general regis When two groups of general registers are a status register bit determines which ge register set bit is addressed.

The PROGRAM STATUS section con the two status registers, the real-time and monitor clock registers, and the inte control circuits. The status registers store gram status information, provide for sele the general register group, enable re from nondestruct read out (NDRO) mer control the disabling of interrupts, and co direct and indirect addressing. The real clock and monitor clock permit the DF monitor elapsed time. The interrupt ci handle program interrupts according to assigned priorities.

The HIGH-SPEED SHIFT and MULTI section contains a shifting matrix and r ply logic that operate without involving ALU of the MPC, and perform tasks than possible in the MPC. The mult logic operates with two multiple digits time.

MEMORY INTERFACE.—The MEM INTERFACE handles the transfer of info tion between the processor/emulator and listing of NDRO bootstrap cards can be found in the AN/UYK-20 User's (Installer's) Manual.

The MEMORY INTERFACE section is divided into three subsections (figure 2-24): MEMORY ADDRESS CONTROL, MEMORY DATA INTERFACE, and NDRO MEMORY (ROM). The MEMORY ADDRESS CONTROL section provides the address information to the main memory. The program address normally increments by one after each memory reference. A breakpoint function allows the program to be stopped when a preselected memory address is referenced. Paging circuits permit the memory to be addressed as 64 separate and interchangeable 1K positions (pages). The MEMORY DATA INTERFACE section transfers data to and from the main memory. The NDRO memory consists of up to 192 words of ROM, which are used for a bootstrap load program.

MAIN MEMORY.—The MAIN MEMORY is a magnetic device that provides storage for the macroprogram. It is available in 8,192-word (8K) increments to a maximum of 65,536 words (65K). As we mentioned earlier, the cycle time is about 750 nsec for a read or write cycle and about 1 microsecond for a read, modify, and restore cycle (referred to as a split cycle). The memory chassis can accommodate up to 12 boards of 3 types of memory: two MCBs, two MDBs, and up to 8 MABs. The MDB, MCB and MAB configurations are as defined in the introductory section on the AN/UYK-20 memory. Two MCBs and two MDBs are always installed on the memory chassis and permit up to 65K of memory.

I/O CONTROLLER.—The I/O CONTROLLER section provides for communication between the AN/UYK-20 and peripheral equipments and includes up to 16 I/O channels (numbered 0-17, base 8). The system provides asynchronous

within a group must
facing characteristics.
duplexed to permit si
mission.

Generally, interfaci
as a shared boundary
devices. Therefore, an
ceived of as an assemb
that make the compute
pheral units. These a
that are distinct from
unit and that may prov
nications. When digit
between two units, the b
levels must be compati
sion is therefore ofter
different types of logic

The I/O CONTR
communication methods
the data exchange betwee
equipments or between
computer. A brief des
munication modes follo

PARALLEL INTE
the general concepts o
in part 1 of this mo
familiar with this conc
the appropriate secti
proceeding with the
Although there are va
types, the three varieties
are as follows:

- Navy Tactical Da
interface uses 0 volts an
binary 1 and binary 0, re
threshold is −6.0 ±
illustrates the output
interface.

- NTDS Fast inte

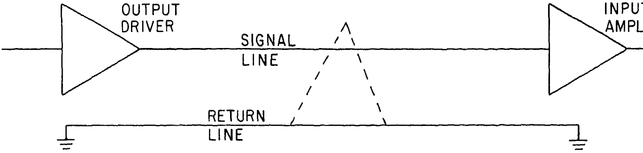


Figure 2-25.—NTDS slow (– 15V) interface.

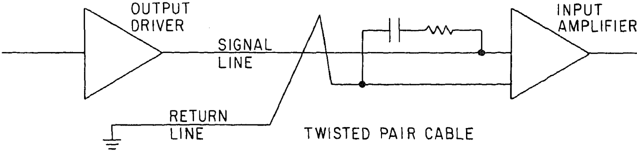


Figure 2-26.—NTDS fast (–3V) interface.

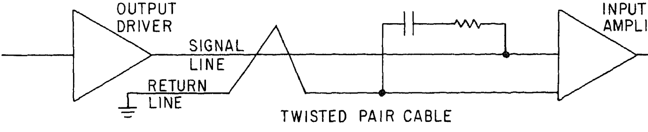
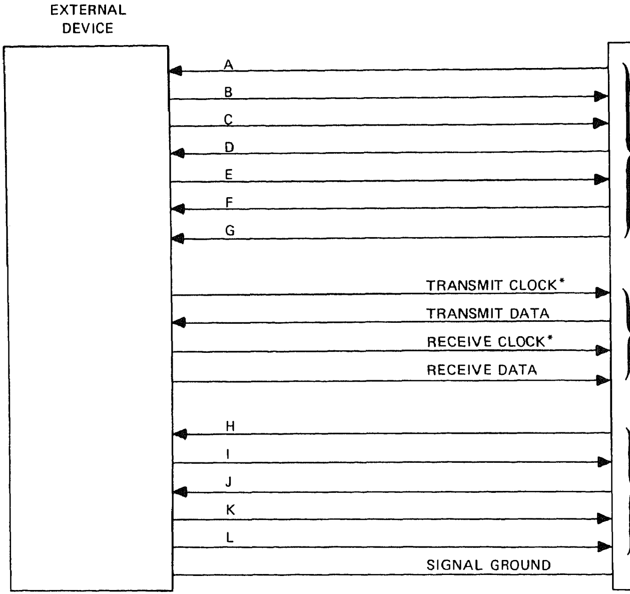


Figure 2-27.—Parallel ANEW (+3.5V) interface.

- ANEW interface uses 0 volts and +3.5 volts to represent binary 1 and binary 0,

following discussion. Although t serial interface types, the var

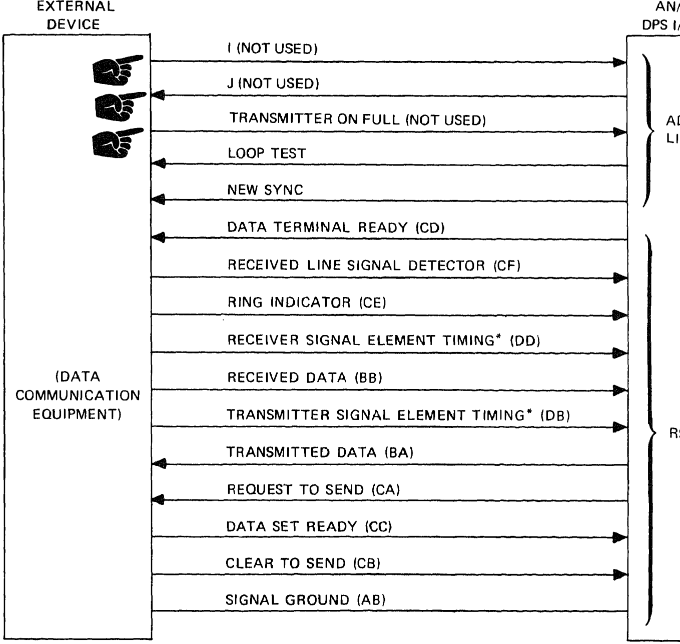


*SYNCHRONOUS MODE ONLY

Figure 2-28.—MIL-STD-188C serial channel interface.

0 volts OFF (figure 2-28). MIL-STD-188C and RS-232C synchronous serial channels provide communications at bit rates up to 9600 bits per second (bps) and require an external clock signal. MIL-STD-188C and RS-232C asynchronous serial channels may have any four of the following modulation rates selective: 75, 100, 300, 600, 1200, or 2400 bps. The four

option. The necessary
standard AN/UYK-20 I/
an enhanced MIL-STD-18
I/O with available charact
It provides four indepen
chronous serial channels.
diagram of the VACAL



NOTE: +6 VOLT = (ON, SPACE, 0)
-6 VOLT = (OFF, MARK, 1) **
( ) = RS-232C IDENTIFICATION
*SYNCHRONOUS MODE ONLY
**EXCEPT FOR LINE J WHICH USES 0 VOLT
INSTEAD OF -6 VOLT FOR THE OFF CONDITION.

Figure 2-29.—RS-232C serial channel interface.

connected at the even-numbered input connector location. The odd-numbered I/O channel con-

The equipment design allow construction that uses a turn-

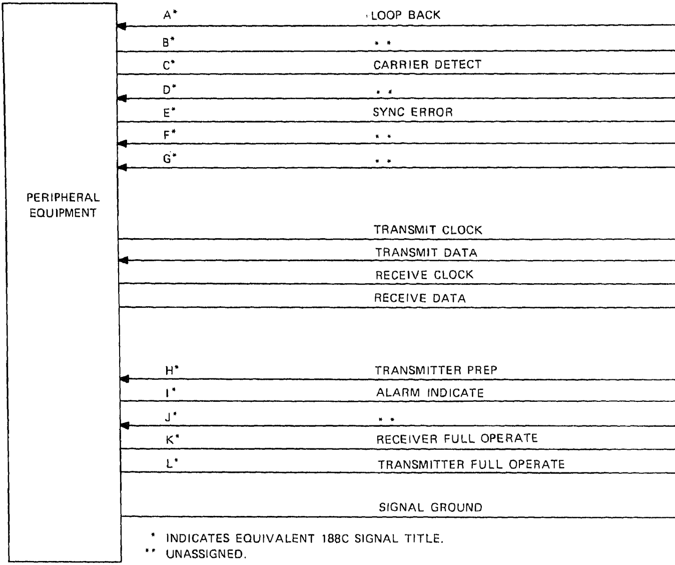


Figure 2-30.—VACALES serial channel interface.

and wiring and timing diagrams. In addition, a built-in maintenance equipment panel is incorporated into the equipment design for use with the software routines to monitor, detect, and isolate failures.

Organizational level maintenance consists of preventive maintenance, system operational checks, troubleshooting, replacement of defective (throw away or turn-in-for-repair) modules and piece-part-repair or replacement of defective

assumption that the majo
will be detected and isolate
various diagnostic test pro
these diagnostic procedure
AN/UYK-20 Technical M
0967-LP-598-1010) Volum

Current maintenance
that diagnostic routines s
periodic basis and when a
suspected or detected. T

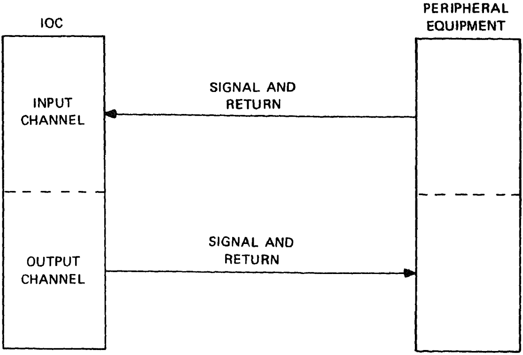


Figure 2-31.—NTDS 32-bit serial I/O channel.

problem is suspected, appropriate supervisory personnel are to be contacted.

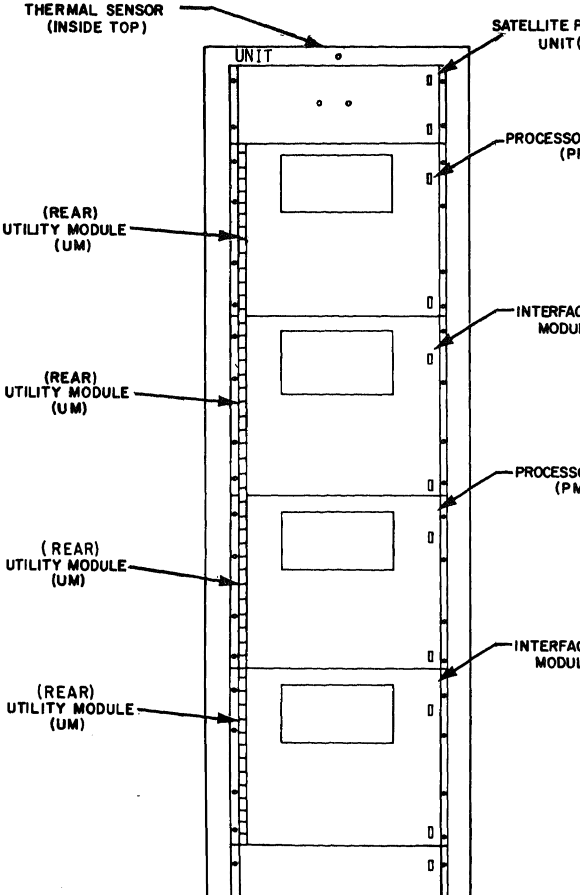
MANUAL TROUBLESHOOTING.—Hardware faults may sometimes prevent the successful loading of diagnostic routines or the successful execution of these routines once they are loaded. One method of troubleshooting in this case involves replacing circuit cards in the suspected area with known good cards until the problem disappears. Another method is to shift multiple usage cards (I/O for example) from one location to another and watch for the problem to shift with the movement of the cards. Extreme caution must be used when shifting multiple-use cards in order to prevent inadvertent damage to operational cards.

Another manual troubleshooting method involves stepping through instructions using the

SYNCHRONOUS DIS
PROCESSOR (

The SDP (figure 2-32) is
time signal processing in a w
cations. For this reason,
primary processor in a vari
within the Ocean Systems c
2-32 is representative of ar
with two processor modul
systems within the Oceanog
may use slightly varying confi
the overall functional con
is the same. The features of
it suitable for a wide ran
are:

- Modularity—The SDP
in either a single or multiple p
tion. All component parts can


THERMAL SENSOR
(INSIDE TOP)
UNIT
SATELLITE P
UNIT(
PROCESSO
(P
(REAR)
UTILITY MODULE
(UM)
INTERFAC
MODUL
(REAR)
UTILITY MODULE
(UM)
PROCESSO
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UTILITY MODULE
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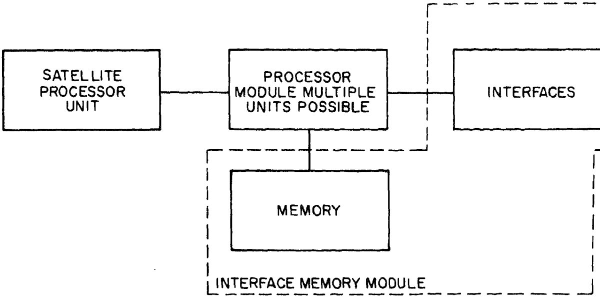


Figure 2-33.—Typical SDP system.

- Unhosted—The SDP operates in a standalone manner and consequently does not require a host computer or another system as a boot device. It can also be "down-loaded" from another computer during software development.

- Complete system—The SDP system generally includes all hardware, software, training aids, and documentation.

SYSTEM COMPOSITION

We will describe a typical SDP system in the next paragraphs. Refer to figure 2-33 as you study the function descriptions.

Satellite Processor Unit (SPU)

The SPU is a Digital Equipment Corporation LSI-11 microprocessor with associated memory interfaces. Its function is to provide the operator-machine interface for system initialization, message processing, terminal interface, performance monitor/fault localization (PM/FL)

composed of a 20-card nest ass
14 to 16 printed circuit cards
programmable subunits:

- Index Arithmetic Unit (
performs process control and g
memory addressees.

- Arithmetic Unit (AU)— T
processor calculations.

- Input/Output Unit (IOU
forms processor I/O functio
control.

The processor module also
interface card, two Erasable
Read-Only Memory (EPROM)
a test and monitor panel. Th
provides a controlled operato
face, and the test and monito
the operator-machine interface
disabled.

INTERFACES.—The interfaces used include standard interfaces such as the NTDS Fast 16 and 32 bit full duplex interfaces, interfaces to Digital Equipment Corporation (DEC), DR-11B and DR-11-C PDP 11 series interfaces, and analog to digital (A to D), and digital to analog (D to A) converters (64 channels each). Any mix of interface cards may be used. The IOU can support up to 30 full duplex interfaces without additional multiplexers.

Utility Module.—The utility module provides power and cooling for both the PM and IMM. The SPU obtains its power and cooling from the utility module used with the PM or IMM, which is located directly beneath the SPU. The utility module connects to the rear of the module it services.

Transformer Connector Assembly.—The transformer connector assembly provides signal isolation and connector mating for external device interfaces.

Cabinet Assembly.—The cabinet assembly provides ac power distribution and overcurrent protection for SDP devices housed in it.

DISTRIBUTED ARCHITECTURE

The distributed architecture of the SDP allows for the breakdown of each complex calculation into several concurrent steps. Five parallel microprocessors in the PM perform the parts of each calculation for many data points at a rate of 8-million instructions per second. (The cycle time of the SDP is 125 nsec.) Results are pipelined, as on an assembly line, to optimize the use of each machine component. Program and data memories are distributed, which enhances the data retrieval rate. The SDP incorporates synchronous design that allows each module to operate at the same clock rate (8 MHz)—thus eliminating the need for software synchronization. Hardware interlocks are also provided.

The modular design of the SDP permits the

memories, and all table memor
EPROM loader. The SPU boots it
stored boot program located in an
in the SPU. During its initialization
internal diagnostics and begins
application programs. The PM/F
program detects the boot conditio
commands to the EPROM loader
SDP programs. The SPU then mor
boot operations and start-up sequer
initialization sequence, the SDP m
through its internal diagnostic pro
beginning its main application pro
after, the SDP regularly checks fo
tions. Detected errors are displayed
indicators and error messages. The
tests operate continuously with e
execution, separated by a predet
interval.

Current SDP configurations m
a degraded mode without the SF
RESET switch of the test and mo
the PM is in the DISABLE posi
operation of the panel control
diagnostics are done manually. Th
an abnormal mode of operation.

Test and Monitor Panel

The test and monitor panel
provides all the controls and indi
line/off-line error monitoring, tro
and some limited aids to program
Figure 2-34 shows the layout o
and indicators of the panel. The
momentary-action/two-position to
and the indicator lamps are light e
(LED). Two 16-position thumbw
are used. The upper switch calls
the REGISTER CONTENT indicat
switch is used to transmit informat
status register when the transmi
SENSE LOAD switch is pressed.

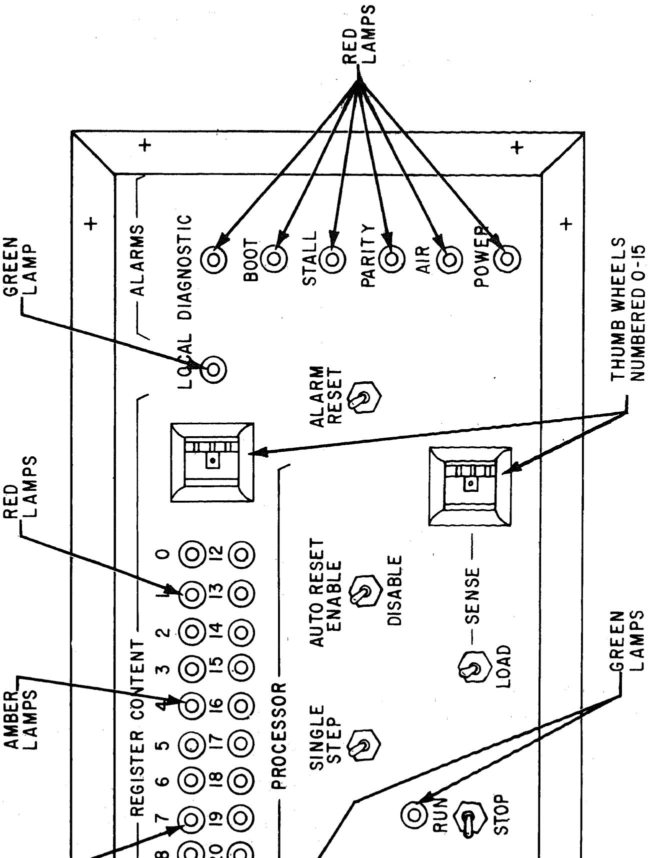

RED LAMPS
GREEN LAMP
ALARMS
LOCAL DIAGNOSTIC
BOOT
STALL
PARITY
AIR
POWER
ALARM RESET
THUMB WHEELS NUMBERED 0-15
RED LAMPS
AMBER LAMPS
REGISTER CONTENT
0
1
2
3
4
5
6
7
8
12
13
14
15
16
17
18
19
20
PROCESSOR
SINGLE STEP
AUTO RESET ENABLE
DISABLE
SENSE
LOAD
GREEN LAMPS
RUN
STOP

Table 2-3.—Processor module controls and indicators

IDENTIFICATION		FUNCT
Control	**Position**	
BOOT-MASTER CLEAR	BOOT	Initiates a boot operat
	MASTER CLEAR	Stops the processor program counters, an PM.
SINGLE STEP	spring return	Advances the processo if previously stopped.
RUN-STOP	RUN	Starts processor opera RUN indicator.
	STOP	Halts processor witho and registers.
AUTO RESET	ENABLE	Enables automatic cor SPU.
	DISABLE	Disables automatic co SPU.
ALARM RESET	spring return	Clears all alarm indic clearing the processor
SENSE LOAD	spring return	Loads the IAU statu value visible on the as switch.
SENSE thumbwheel switch	0-15	Selects the value to be status register.
REGISTER CONTENT thumbwheel switch		Controls the data to REGISTER CONT follows:
	0	IAU status register
	1	IAU: Index, Cont memory diagnostics

Table 2-3.—Processor module controls and indicators—Continued

IDENTIFICATION		FUNCTION
Control	**Position**	
	6	IOU parameters
	7	IOU status
	8-15	Program Dependent
Indicator	**Color**	
LOCAL	Green	Indicates that the R CONTENT thumbwheel controlling the REGISTER indicators.
BOOT	Green	Indicates that a boot ope progress.
RUN	Green	Indicates that the processor i
DIAGNOSTIC	Red	Indicates the presence of softw errors. The errors have been panel registers 8-15.
BOOT	Red	Indicates that the EPROM mi has detected a boot error.
STALL	Red	Indicates that the IOU has de error that has not beet corr SPU.
PARITY	Red	Indicates that a parity error in one of the processor memo exception of working and memories.
AIR	Red	Indicates insufficient airflo processor utility module.
POWER	Red	Indicates that one or more of supplies in the processor ut have failed or "crowbarred,"

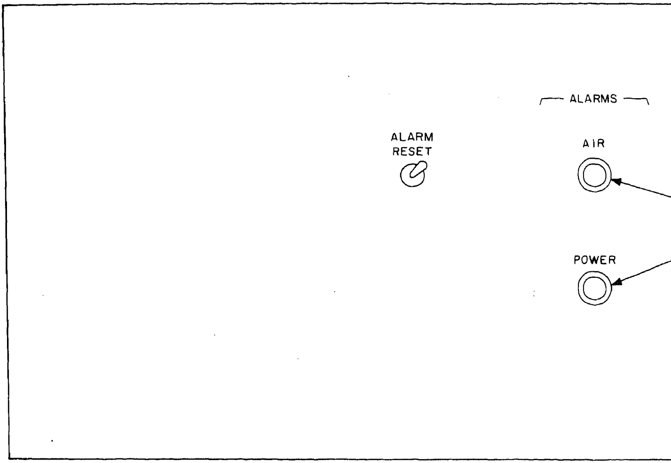


Figure 2-35.—Interface—memory module, control panel.

Table 2-4.—IMM controls and indicators

IDENTIFICATION		FUNCTI
Control	**Position**	
ALARM RESET	Spring return	Manually clears the ala
Indicator	**Color**	
AIR	Red	Indicates insufficien associated utility modul

Interface Memory Module (IMM)

The IMM contains operand and/or buffer memory cards, some IOU interface cards, and a control panel. Figure 2-35 shows the layout of the controls and indicators of the IMM control panel. Table 2-4 shows the functions of the controls and indicators.

Satellite Processor Unit (SPU)

The control panel of the

figure 2-36. Table 2-5 provides

the controls and indicators.

Power and Control Panel

The power and control pa

contains the main cabinet pow

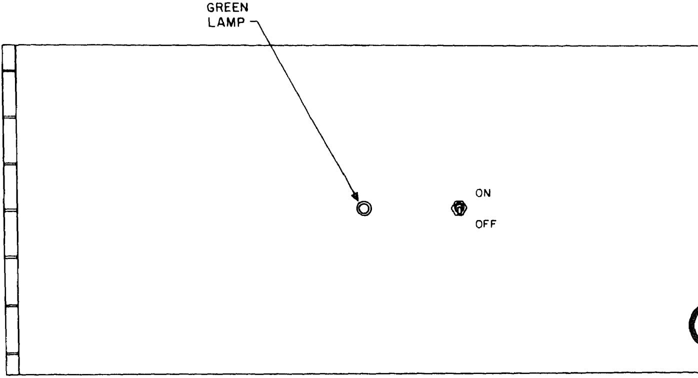
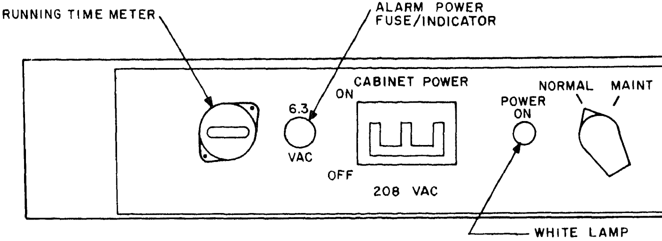


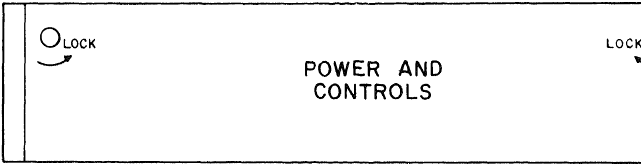
Figure 2-36.—Satellite Processor Unit, control panel.

Table 2-5.—SPU control panel switches and indicators

IDENTIFICATION		FUN
Control	Position	



COVER OPENED



COVER CLOSED

Figure 2-37.—Power and control panel.

overcurrent protection. The panel also contains a power indicator, fuse and blown fuse indicator (6.3V), time meter, and a maintenance switch. Table 2-6 shows the functions of the controls and indicators.

BASIC OPERATING PROCEDURES

The operating procedures for the SDP include an automatic start-up mode (normally associated with a fully operational SDP) and several manual modes of operation. Manual start-up procedures are incorporated to allow continued

SDP initiates the automatic star
the sequence is because of mo
loss or software (program) co
ator intervention is required. I
sequence is because of an inte
of cabinet or module power, a sta
procedure must be followed.
(program) applications may re
operation actions. In these case
dures can be found in the appro
manuals.

Table 2-[illegible]. Power and control panel switches and indicators

IDENTIFICATION		FUNCT
Control	**Position**	
CABINET POWER 208 VAC	ON/OFF	Controls ac power to al cabinet, except utility
NORMAL-MAINT	NORMAL	Enables all cabinet and alarms.
	MAINT	Disables cabinet and re
Indicators	**Type**	
POWER ON	White Lamp	Indicates that ac power cabinet.
RUNNING TIME INDICATOR	Digital meter	Indicates the total oper the cabinet in hours.

Manual Test Mode

In the manual test mode, the processor can be started and stopped by the operator or single stepped through the program or test. In this mode the AUTO RESET switch disables all SPU automatic features, such as boot of memories, master clearing, resetting of alarms, program clearing of the IAU status register, processor start, and control of the processor.

Operator Turn-Off

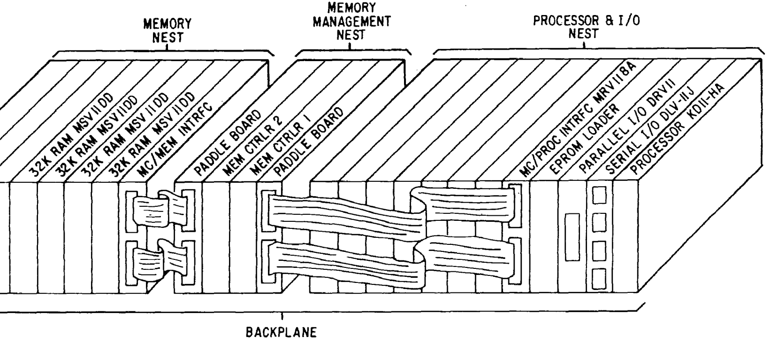
Power to the SDP is secured by means of the CABINET POWER 208 VAC switch on the power and control panel. When the 208 VAC switch is placed in the OFF position, power is

VAC switch. THIS ACTIO
REMOVE LINE VOLTAGE
FRONT AND REAR UTILITY

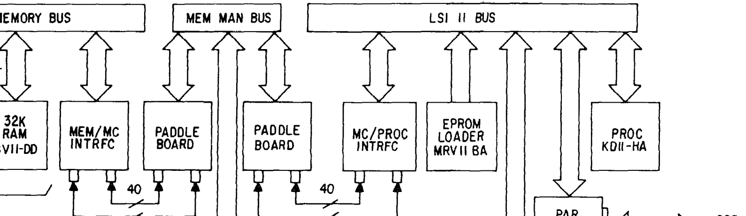
FUNCTIONAL DESCRIPTIO

The following paragraphs
overview of the components of
intended to expand the explar
outlined in the introductory se
explanations of SDP componen
in manufacturer technical manual
application manuals.

Satellite Processor Unit (SPU)



PHYSICAL/FUNCTIONAL SPU CONFIGURATION



been removed. A typical SPU configura- is shown in figure 2-38. In the next raphs we will give a brief explanation of ajor DEC modules that commonly comprise PU.

D11-HA MICROCOMPUTER PROCES-—The KD11-HA is a 16-bit microcomputer direct addressing of 32K 16-bit words or 3-bit bytes. For this application, an option d to provide an extended and floating point action set. Other features of the micro- uter are a 380 nsec microcycle time, single- double-operand instructions, and PDP-11 tern Electric trademark) software compati- .

LV11-J FOUR-LINE SERIAL INTER- E.—The DLV11-J is a four-channel asyn- nous serial line unit used to interface heral equipment to an LSI-11 bus. Each nel on the module can act as an independent face and can be configured separately for and data bits, parity, and baud rates (up to 0 baud). The fourth channel has the lowest ity interfaces with a console terminal cally a TermiNet T1200 teleprinter). Data mission between the peripheral device and nterface is over a "data leads only" EIA rnal interrupt acknowledge) configuration, n does not use control lines.

RV11 16-BIT PARALLEL INTER- E.—The DRV11 is a general-purpose face unit used to connect parallel line istor-transistor logic (TTL) devices to the 1 bus. Program-controlled data transfer up to 40K words per second are permitted. PU applications, the DRV11 provides the face to one or more associated SDPs (one 11 per SDP). An SPU/IAU interface des buffering between the systems.

ISV11-DD DYNAMIC MOS RANDOM ESS MEMORY (RAM) MEMORY.—The

H9281 MICRO BACKPLANE.—The is a family of backplane assemblies us support the LSI-11 modules. These asser provide the embodiment of the LSI-1 termination and power connectors.

SPU Memory Management (Internal)

The internal memory management s for the SPU is diagrammed in figure 2-3 has the following features:

- Two sets of page registers are pro one for use in the operating system (mode) and one for use in the appli program (user mode).

- The active set of page registers is mined by the contents of a new user/ mode register. Switching between kerne user modes is strictly a software function

- Memory management status re SR0 and SR2 are provided.

- An external interrupt is generated memory management fault.

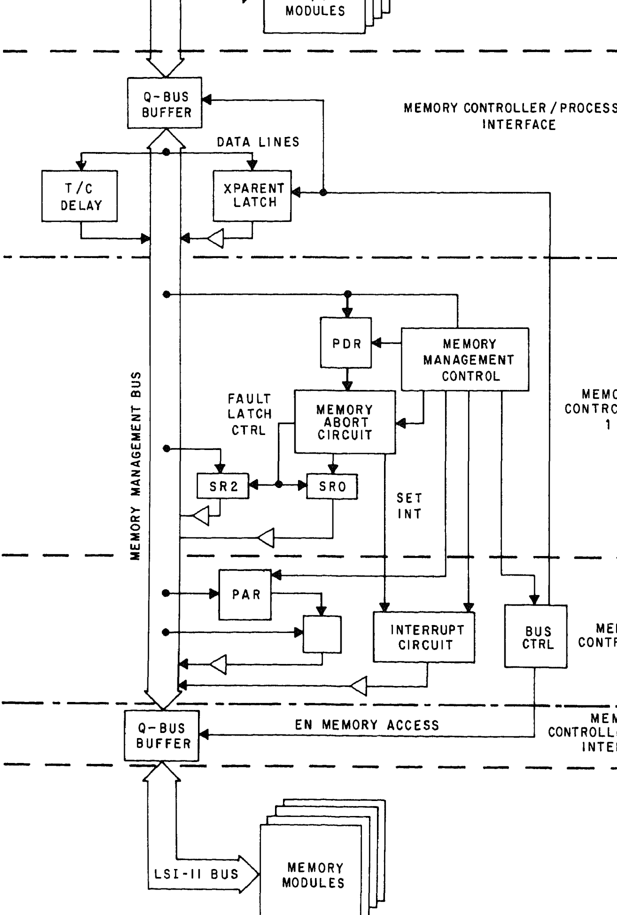
- I/O operations are not mapped th memory management.

- All 128K words of physical memo available.

Memory management in the LSI-1 implemented by extending the LSI-11 bus th a nest containing all memory manag circuitry to a nest containing only memo

MEMORY CONTROLLER/PROCE INTERFACE.—The circuitry on the m controller/processor interface board pr the buffering to isolate the memory manag section bus from the processor and I/O s bus. This interface is bidirectional.

MIRROR IMAGE CABLE CON TOR.—The mirror image cable connecto


MODULES
Q-BUS BUFFER
MEMORY CONTROLLER / PROCESS
INTERFACE
DATA LINES
T/C DELAY
XPARENT LATCH
PDR
MEMORY MANAGEMENT CONTROL
FAULT LATCH CTRL
MEMORY ABORT CIRCUIT
MEMORY MANAGEMENT BUS
MEMO
CONTRO
1
SR2
SR0
SET INT
PAR
INTERRUPT CIRCUIT
BUS CTRL
ME
CONTR
Q-BUS BUFFER
EN MEMORY ACCESS
MEM
CONTROLL
INTE
LSI-II BUS
MEMORY MODULES

IEMORY CONTROLLER 2.—Memory
roller 2 contains the 16-page address registers
Rs), memory management abort (interrupt)
, and controls for the direction of data
fer.

INE TIME CLOCK.—The line time clock
des a clock signal to the SPU in the form
interrupt at a 60-Hz rate. The clock signal
rived from a 6.3 Vac 60-Hz source and is
by the SPU for scheduling and task switch-
The SPU will not operate without this clock.

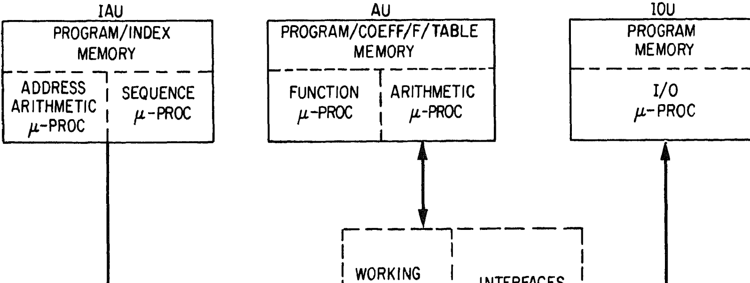
S-232C OPTICAL INTERFACE.—The
al interface is available as an option to isolate
S-232C line connected to the SPU. Power
red to operate the outboard side of this
e is derived from the SPU main power source
gh isolated dc/dc converters. This interface
ated between the DLV11-J (four line serial in-
ce) and the peripheral RS-232C equipments.

PU/IAU INTERFACE.—The SPU/IAU in-
ce contains buffer/multiplexer circuits. These
its allow a single 16-bit parallel I/O port
/11 16-bit parallel interface) in the SPU to
face with a variety of data ports in the SDP.
into 16-bit words for transfer to the SP
DRV11 interface in the SPU. The SPU
interface provides all the required handsh
signals to both the DRV11 and the EP
loader. Control of this interface is throu
boot software in the SPU.

SDP FRONT PANEL INTERFACE.—
test data representing the contents of a se
test register in the SDP and serial error dat
the SDP front panel are transferred to th
via the test and error data buffer of the SPU
interface. Serial test data are 24 bits in lengt
serial error data is 8 bits. Both of thes
sources are via the SDP front panel. The SP
select the SDP status register to be transfer
serial test data. The SPU can also control
SDP front panel functions such as start,
master clear, and error reset through the r
control portion of the SPU/IAU interfac

Processor Module (PM)

The PM of the SDP system (sometimes
the SDP proper) is a highly parallel, highly
lined signal processor. It consists of thre
grammable units (see figure 2-40) each of



executes its own program. These units are the Index Arithmetic Unit (IAU), the Arithmetic Unit (AU), and the Input/Output Unit (IOU). Instructions are executed at a rate of 8-million instructions per second, which makes for an instruction execution time of 125 nsec. Since there are no instructions that take multiple cycle times, each instruction executes in this interval. Among the three units that comprise the PM are five bipolar microprocessors that operate in parallel. This results in a total of 40 million microprocessor instructions being executed per second.

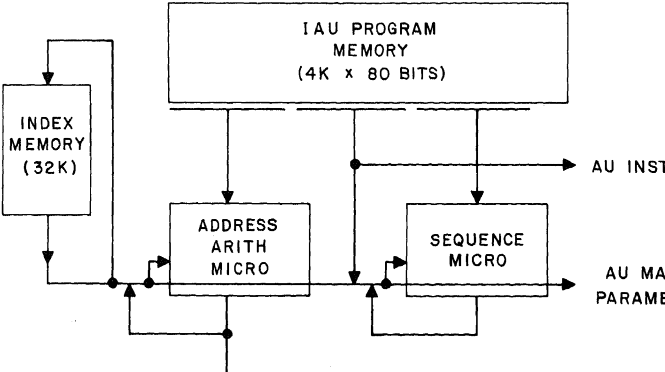
Briefly defined, the IAU exercises overall algorithm control and is responsible for generating addresses for the working memory. The AU is the arithmetic processor part of the SDP and receives data from the working memory. The IOU performs arithmetic and logic operations on the data and sends the data to the working memory and the IOU. Each of these units is programmed independently of the other once structured into control flow, arith and a template of I/O activity.

The IOU serves as the interf synchronous AU and IAU an outside environment.

Interactions among the IAU are, for the most part, controlle that keep the flow of data and c sistent. However, there are insta IAU and the IOU must check con their respective status registers whether a data transfer is to tal

The following discussion dev each unit of the PM and is inter your comprehension of the theor More specific details can be four facturer handbooks and technic

INDEX ARITHMETIC UNI IAU (figure 2-41) is a program



- The control memory stores the program he IAU.

- The index memory holds data for se- cing the program and generating working ory addresses.

- The address arithmetic microprocessor M) performs the address calculations for ing memory.

- The sequence microprocessor controls ram sequencing operations.

- The memory address pipeline performs unction of cyclic addressing and queuing of in addresses.

- It facilitates the interfaces to the SPU, and IOU

the AU section of the PM. The AU is com of the following segments, which perfor functions indicated:

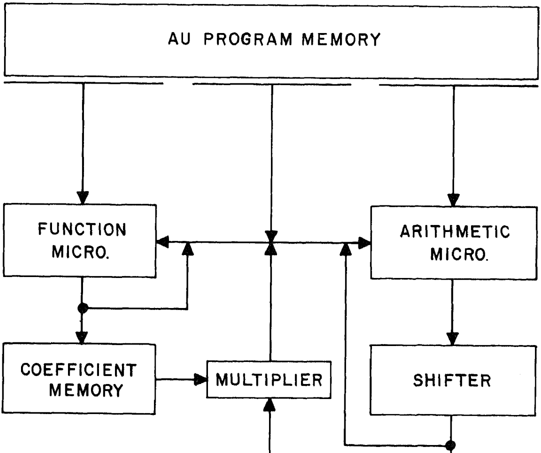
- A coefficient memory for the stor fixed processing parameters and constant

- A table memory used as an in lookup table for the coefficient memory.

- A FRAM memory, which is a scrat memory.

- A function microprocessor whose task is to generate addresses for the coeffi table, and FRAM memories.

- The arithmetic microprocessor fun as a set of accumulators and performs l operations.



for communication among the three busses of the AU.

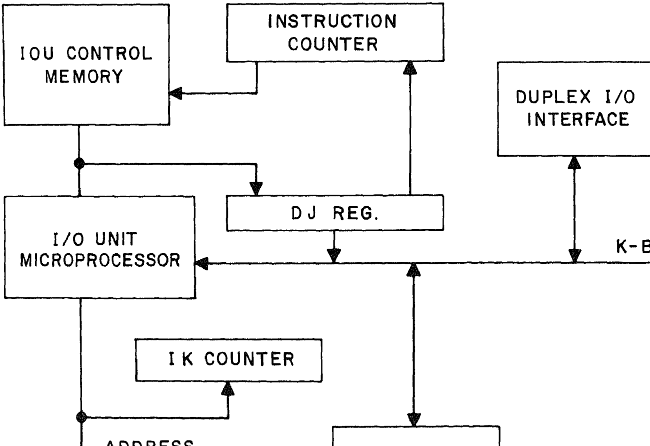
- A combination shifter, which can shift a data word left or right by up to 16 bits in a single machine cycle.
- Rounding logic to supply appropriate rounding for two's complement arithmetic.
- Complex threshold logic for estimating the magnitude of complex numbers.
- A most significant digit encoder for determining how far left or right to shift a number to normalize it.
- Communication paths with the IAU, IOU, and working memory.
- A status register.

INPUT/OUTPUT (IOU) Unit.—The IOU consists of a single I/O microprocessor (IOM),

The principal task of the I
data for the input and outpu
include merging the output from
received on input ports so as to
output data stream. Some exam
trolling of accesses to an exte
system, the providing of storag
arrays of intermediate results i
memory, and the transmitting
other SDPs as well as relaying it
examples are the checking for
pulses on sample streams, and,
configured, demultiplexing.

EPROM LOADER-SDP BOOT SERVICE

The EPROM loader system
SPU consists of an EPROM
and an optional EPROM load
EPROM loader 1 board cont



circuits for "booting" both the SDP and the SPU as well as 128K bytes of storage. The EPROM loader 2 board contains an additional 256 bytes of storage.

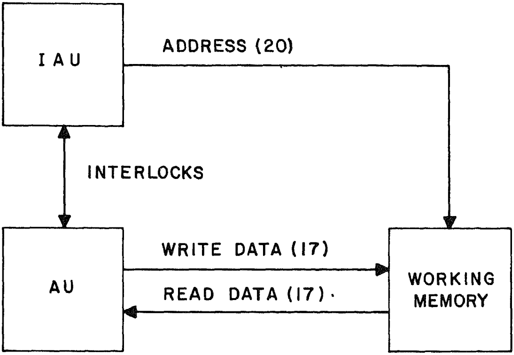
EPROM Loader Purposes and Functions

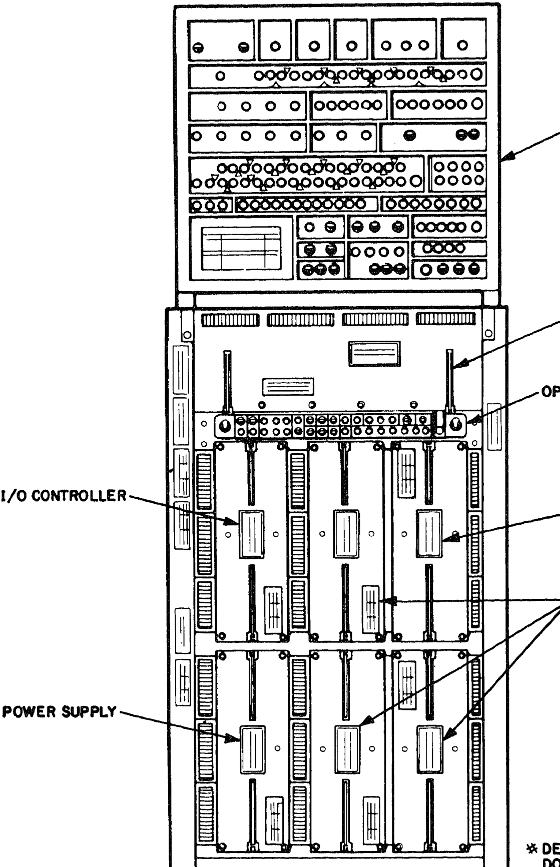
The EPROM loader 1 board, in normal system operation, receives control information from the SPU via the SPU/IAU interface card. This control information is a 4-bit code, which tells the EPROM loader 1 board which of 16 possible programs to load. These programs can be either SPU programs or PM programs. If the SPU fails to function properly, it is still possible to boot the PM by means of a switch setting on the EPROM loader 1 board, which is accessible from the front of the board. This switch setting tells the EPROM loader 1 board which program to boot.

The EPROM loader 1 board verifies all data read from the EPROMs on the EPROM loader 1 and EPROM loader 2 boards. Er
to both the front panel of the PM
The EPROM loader 1 board als
verification of all data that
the PM at boot time. Any erro
also reported to both the PM fr
the SPU. The SPU does its own
loaded into the SPU from the
This makes it unnecessary for th
1 board to do a readback verif

INTERFACE MEMORY MOI (IMM) BULK MEMORIES

The SDP system incorporat
semiconductor RAM system wi
8-million words per second, wh
operand and I/O buffer functi
and dynamic RAM technologies
and can be mixed in various pro
2-44 is a block diagram repre




OP
I/O CONTROLLER
POWER SUPPLY
✲ DE
DO

Working Memory

Working memory (referred to as main memory or operand memory) is addressed by the IAU. The address field is 20-bits wide, which is required to address 1M (1,048,576) words. Working memory receives write data from the AU and returns read data to it. These data paths are 17-bits wide, with one bit used for parity error checking.

I/O Buffer Memory

The I/O buffer memory (also called buffer memory) is addressed by the IOU. This address field is 20-bits wide (same as working memory). The read and write data paths out of and into the buffer memory are 17-bits wide, with one bit being used for parity error checking.

IMM Memory Organization

Memory cards (working memory and I/O buffer memory) are housed in the IMM and can consist of from 1 to 64 circuit cards, depending on the type and amount of memory needed. The minimum static memory consists of one 65K RAM card. The maximum system consists of 64, 16K cards filling three complete IMM and part of another (20 cards for each IMM). The minimum dynamic system consists of one 65K controller and one 65K RAM. The maximum dynamic system is one controller and 16, 65K cards.

The IMM backplane (rear of unit containing card connectors, cables, and so forth) is organized in such a way that it can be easily portioned to handle several functional blocks of various sizes, depending on specific SDP application requirements. For example, a 20-card IMM can be configured for a 6-card working memory, a 9-card I/O buffer memory, and 5 cards dedicated to I/O functions, such as digital to analog (D/A) or analog to digital (A/D) conversions. For the most part, backplane connections are

used in the Target Data Proces
the Ocean Systems community

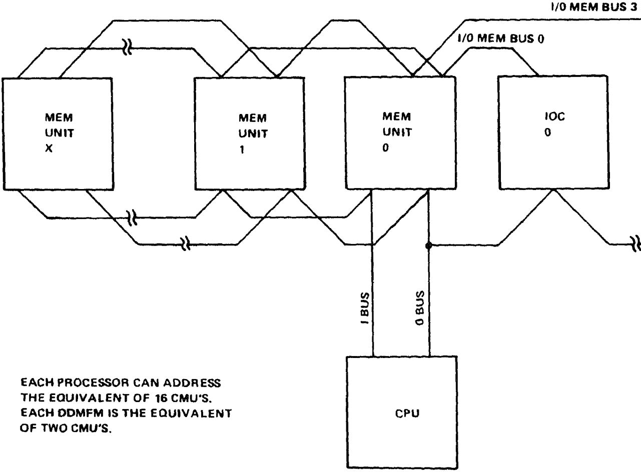
The AN/UYK-7 is a genera
computer with a multiprocessi
allows a number of central pr
operate at the same time in t
Communication between the C
and I/O controller is via a b
tions system consisting of thre
instruction, operand, and I/O
faces with the memory units
These busses consist of connecti
the CP, memory units, and I
cable connections. There are 4
bus with a total of 32 cable
accesses to any 1 memory unit.
arranged as shown in figure 2
bus connects the CP and a pa
unit; for example, memory uni
0, in turn, is connected to me
and so forth, up to core mem
maximum computer configura

The computer has the follo
tion capabilities between units

- Each CP can address the
to 16 core memory units and co
I/O controllers. Each cabinet
one CP unit.

- Each I/O controller uni
equivalent of up to 16 core m
communicates with external de
I/O adapter. The I/O contro
trolled by a maximum of thre
Each cabinet can contain onl
troller.

- The I/O adapter can co
external devices via input and
which are provided in multipl
I/O adapter has 4, 8, 12, or 1
cabinet can contain only one I



EACH PROCESSOR CAN ADDRESS THE EQUIVALENT OF 16 CMU'S. EACH DDMFM IS THE EQUIVALENT OF TWO CMU'S.

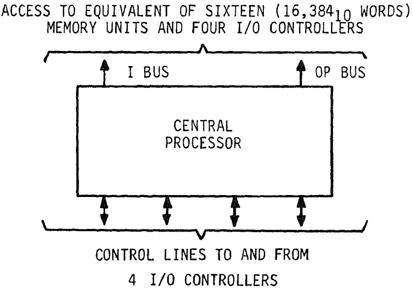
Figure 2-46.—Central processor communication system.

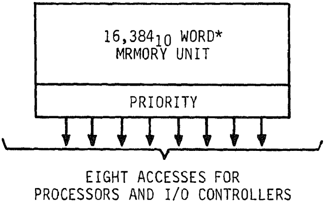
The interface combinations between units of the computer are illustrated in figure 2-47.

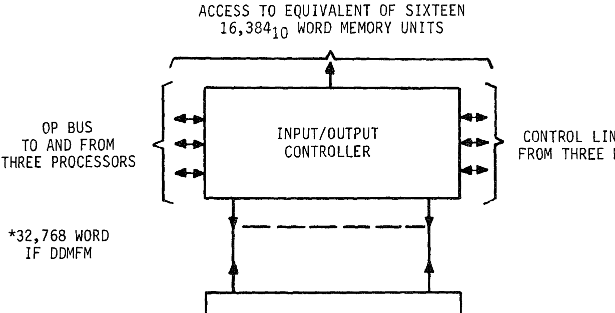
Interface timing between computer units is handled on an asynchronous basis. Data transfers are performed via a request/acknowledge system (handshaking). Each unit (including the arithmetic and control sections of the CP) contains its own separate timing sources.

The computer contains three types of memory: main memory, control memory, and nondestruct read out (NDRO) memory. Main memory is a destruct read out (DRO) memory consisting of three 16,384-word core units or three 32,768-word double density mated film memory (DDMFM) units. These figures refer to a single

operations. The control me
flip-flop storage registers th
each. The control memory
stores data used for operanc
tion, interrupt execution,
update operations. The ND
of 512_{10} or 1024_{10} words.
is contained in the CP and i
of programs fabricated as
the CP. The purpose of N
provide a means of auton
DRO memory and to provic
analysis and load-failure
NDRO memory contents ca
specifications.


ACCESS TO EQUIVALENT OF SIXTEEN (16,384$_{10}$ WORDS) MEMORY UNITS AND FOUR I/O CONTROLLERS
I BUS
OP BUS
CENTRAL PROCESSOR
CONTROL LINES TO AND FROM
4 I/O CONTROLLERS





*32,768 WORD
IF DDMFM

contained in the NDRO module must be preprogrammed for each specific type of peripheral equipment and channel assignment.

The hardware fault analysis program identifies hardware fault conditions to ensure that the system can recover from hardware error interrupts. Working with the NDRO hardware fault analysis program, this program requires that the computer system have a normal recovery program and an alternate recovery program for the hardware error interrupts. The normal and alternate recovery programs should not be stored in the same memory bank.

The normal recovery program is part of the executive program. If the hardware error interrupt indicates no memory failure, the normal recovery program is executed. If the interrupt indicates a memory failure, the alternate recovery program is executed, unless the alternate recovery program is in a failed memory bank. In this case a normal recovery is executed.

The purpose of the load-failure analysis program is to aid maintenance personnel. This program provides diagnostic-type isolation under conditions where loading of the DRO memory cannot be accomplished by the bootstrap programs or by manually aided I/O controller techniques. A load failure exists when a computer hardware fault prevents the loading of the DRO memory. This program occupies about 360_{10} words of NDRO memory.

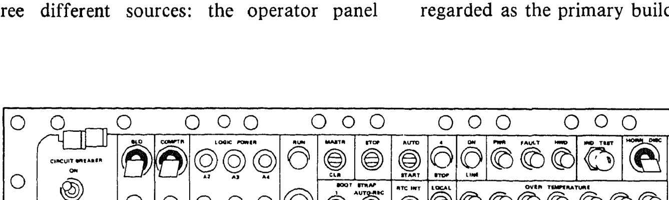
Computer operations can be controlled from three different sources: the operator panel

computer operation under prog
maintenance console is usec
maintenance purposes. The
initiates and monitors com
from a remote location. The
remote consoles are not req
operation.

A typical AN/UYK-7 si
bay-configured computer is
2-45. The AN/UYK-7 is desig
a single- or multiple-proce
AN/UYK-7 single-cabinet cor
tion consists of the following

- One central processor.
- One I/O controller.
- One I/O adapter (16 interface I/
  options (16 parallel I/C
  (12 parallel, 4
- One power supply unit
  Options (115 V)
  (208 V)
- Three memory units (core mer
  words each)
  (double density mated film mer
  (32K) words each).
- One test set (maintenance conso
- Operator's console.
- One computer control unit (rem
- One electrical equipment cabine

The basic single cabinet
regarded as the primary builc



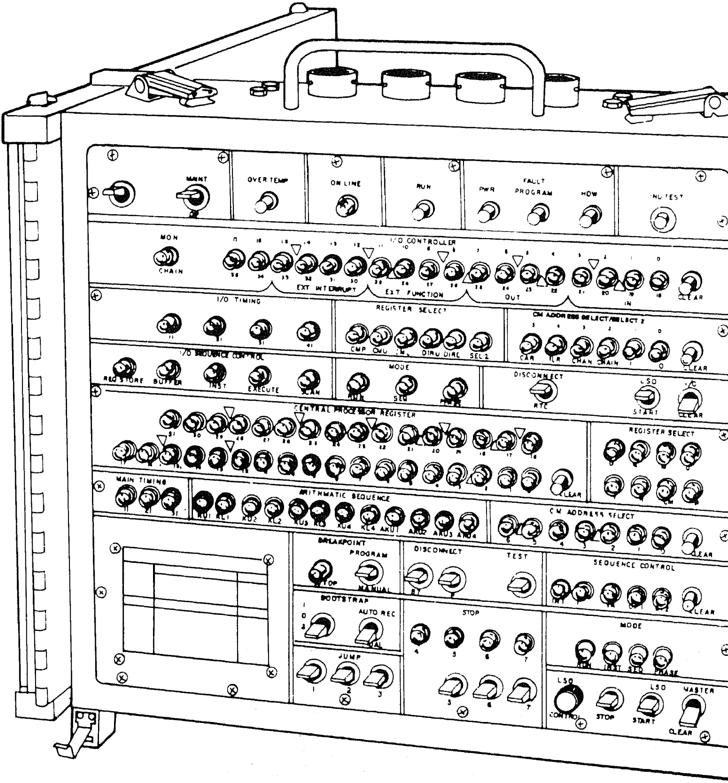
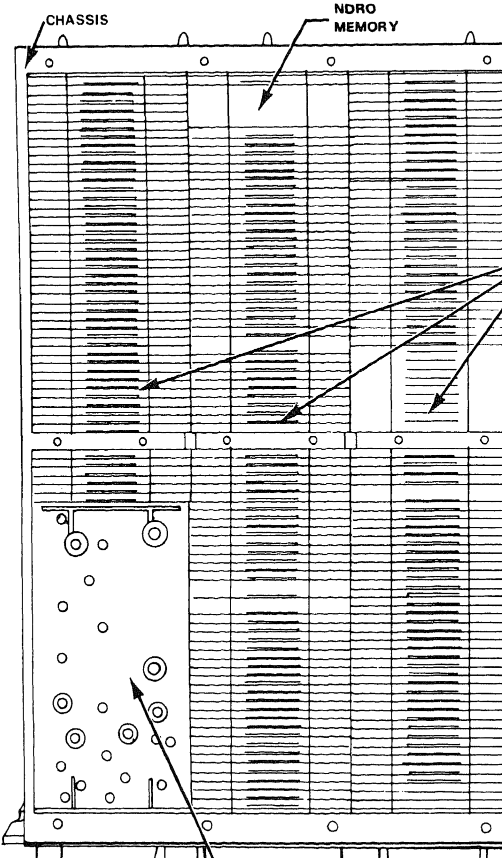


Figure 2-49.—Maintenance console.


CHASSIS
NDRO MEMORY

TRAL PROCESSOR (CP)

he CP (figure 2-50) controls the overall tion of the computing system. It contains e control (excluding control of peripheral ments), arithmetic, and timing circuitry to ss data. The CP can address up to 16 ory units. Instructions are obtained from memory units via a communications bus instruction or I bus (see figure 2-46). ands are obtained and stored via another munications bus called the operand or O The O bus transfers data between I/O ctors (IOCs) (maximum of 4) and the CP. CP operates as an independent unit with its power distribution, timing, and so on. Only P can be mounted within any one cabinet.

he CP consists of 201 individual modules, nodule package compressing the NDRO ory, a dc-to-dc converter and the accompany- hassis. Each individual module is placed the chassis via a 56-pin connector. The O memory module package is equivalent in ness to five individual modules and is ed into the chassis via three rows of 56-pin connectors. Cooling is provided by a r in the bottom of the cabinet that forces rough a ribbed heat exchanger plate. The exchanger plate, along with a chassis cover, also provides radio frequency (RF) ing.

CONTROLLER

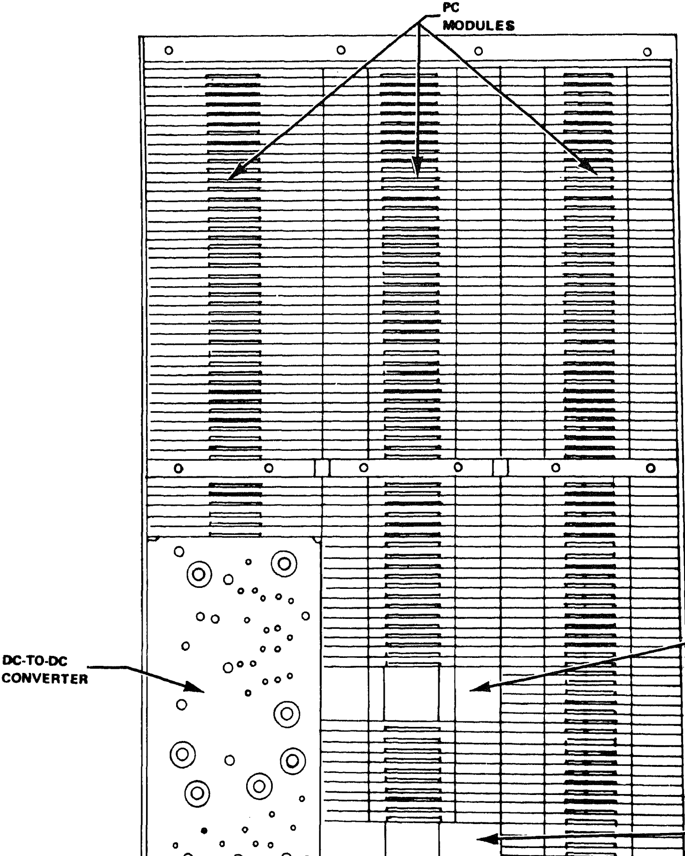
ith the exception of the guide pin locations unit/cabinet interface, the I/O controller re 2-51) is dimensionally equivalent to the The I/O controller controls the transfer of between the main memory and peripheral ment of the computer. Data and control ls are exchanged with the peripheral equip- s via the I/O adapter. The I/O controller ams are initiated by instructions from the nd executed by a series of I/O controller

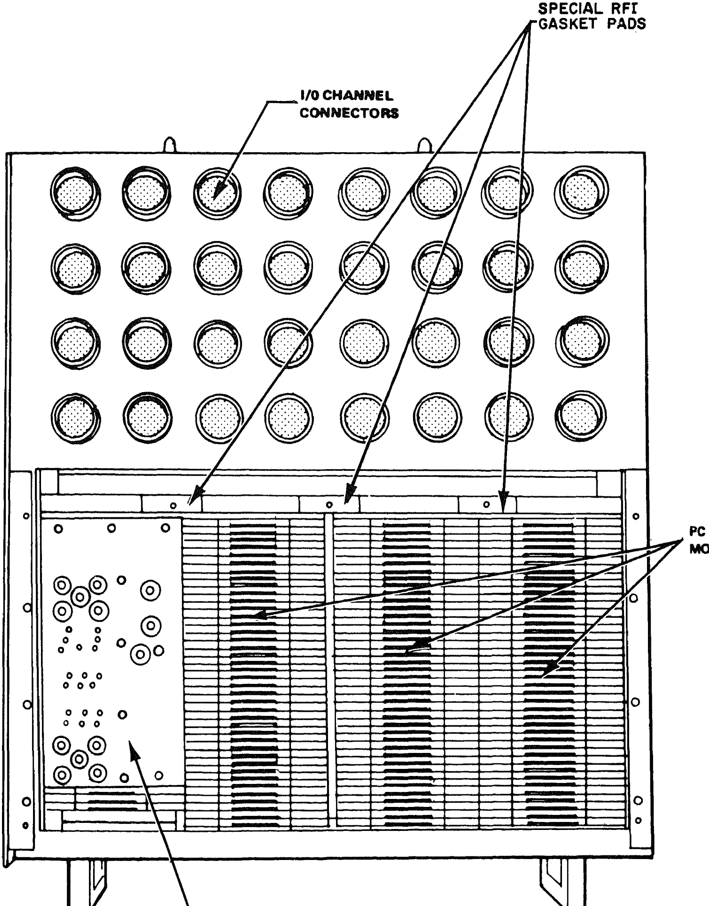
voltage requirements of the computer o pheral equipment. The I/O adapter cons 16 I/O channels (32 connectors) arrang groups of four I/O channels. Each gro 4 I/O channels uses either a fast int (−3.0 volts or +3.5 volts), a slow int (−15 volts), or a serial interface (bipolar volts to −3.0 volts). The I/O adapter re data and control signals from the I/O con logic of the computer and returns dat acknowledge signals to the I/O controller The I/O adapter also transfers data and c signals to the peripheral equipment and re data and acknowledge signals from peri equipment.

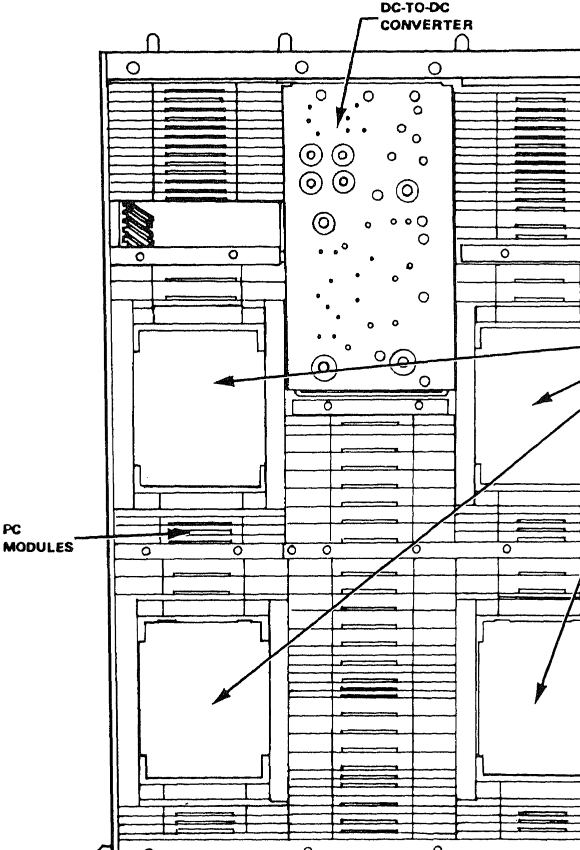
The I/O adapter contains 122 modu dc-to-dc converter, 32 I/0 channel conne and the accompanying chassis. The unit is in horizontally into the top area of its c above the operator panel. The unit is d into two halves: the front half, which co printed circuit modules and the rear half, contains I/O channel connectors for hool peripheral equipment. A heat exchanger is s over the top of the front half and dissipate from all printed circuit modules.

MAIN MEMORY

Each main memory unit contains sel circuits, control circuits, timing circuits, distribution wiring, and interface conn facilities. These devices enable main mem communicate with the I/O controller an The primary function of main memory store programs or data. The main memory may be one of two types: core memory u DDMFM units. Each DDMFM chassis ha the capacity of a core memory chassis (32 versus $16,384_{10}$ words), hence the term "d density." The maximum addressable m for a system with one central processor rem $262{,}144_{10}$ words and may be formed b


PC MODULES
DC-TO-DC CONVERTER


SPECIAL RFI GASKET PADS
I/0 CHANNEL CONNECTORS
PC
MO


DC-TO-DC CONVERTER
PC MODULES

esignated 0, 2, and 4, respectively. (DDMFM quivalent to core memories 0 and 1, and so The memory units (figures 2-53 and 2-54) in the following components.

- Core Memory Unit—77 printed circuit ules, four plugged 4K memory stacks, and a -dc converter.

DDMFM Unit—89 printed modules, two ;able 16K memory stocks, and a dc-to-dc erter.

VER SUPPLY

he power supply (figure 2-55) converts ary power to regulated −90-volt power red for the dc-to-dc converters of the unit urnishes regulated voltages for the operator and computer cabinet. The power supply generates master clear and interrupt signals ponse to operator panel control and voltage, nt, and temperature out-of-tolerance condi- . If power fails, the power supply has gh stored energy to supply the computer for microseconds; enough time to store all ile information. The unit consists of chassis-mounted components and plug-in ules. The power supply is cooled by forced rough a ribbed heat exchanger.

NTENANCE CONSOLE

he maintenance console enables personnel perate the computer under expanded and d conditions and at various speeds and s of operation. Maintenance personnel tor instruction words and their operations, metic registers, control registers, and g. Various faults and overtemperature itions can also be monitored. The mainte- e console (figure 2-49) can be mounted in kets on top of the computer cabinet or

enables the operator to apply computer a dc power, start and stop computer opera observe fault and overtemperature cond apply dc power to the maintenance consol test indicator/audible alarm capability. controls and indicators consist of toggle sw incandescent indicators, and combination button neon indicators.

COMPUTER CONTROL UNIT (REMOTE CONSOLE)

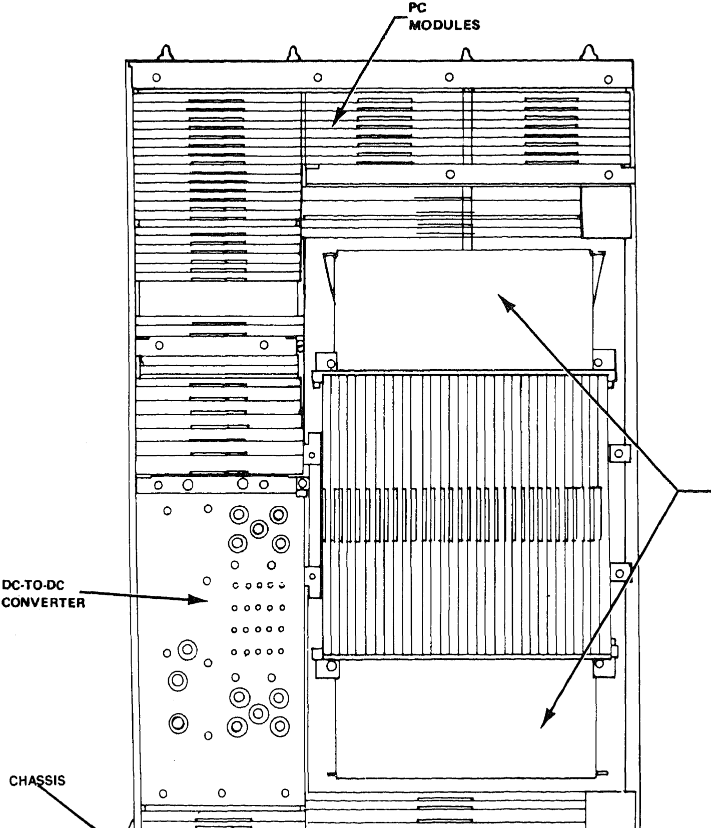
An optional computer control unit called a remote console) enables the opera control computer operations. The remote c can be located up to 300 feet from the com The unit has basically the same capability operator panel, with the exception that application is not possible from the r console. However, the remote console ON control switch can override computer c from either the operator panel or mainte console when computer power has been a from the operator panel.

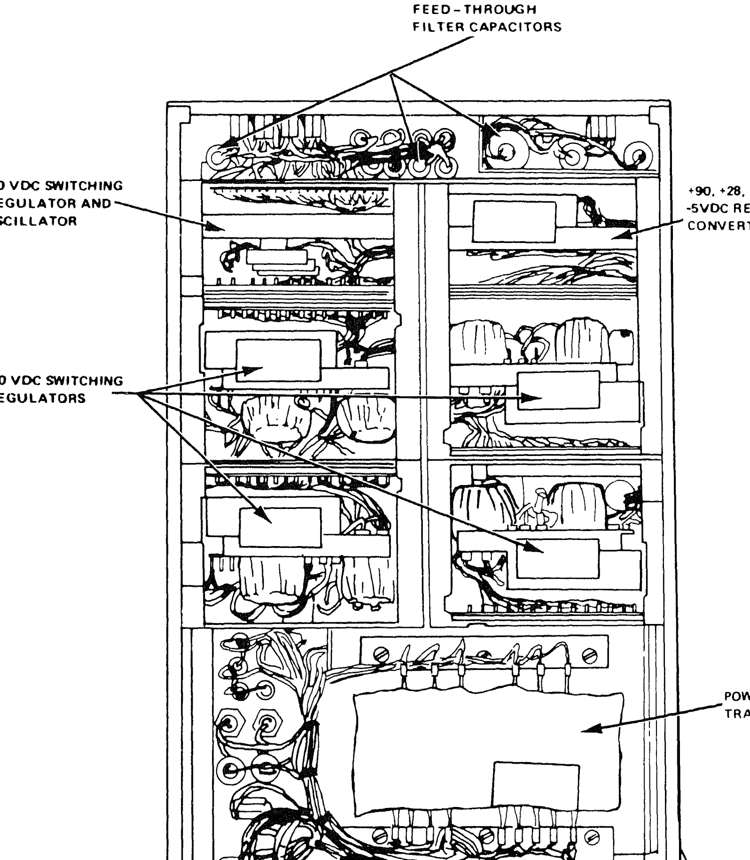
COMPUTER CABINET

The computer cabinet consists of a v frame that can accommodate one I/O a module and six common-size modules cabinet contains module mounting slide retaining hardware, module electrical conne and interconnecting wiring harnesses. I contains an operator control panel, a b and a system of air ducts to allow cooling circulate throughout module heat exchan

SUMMARY

We discussed the physical makeup AN/UYK-20 computer at the beginning


PC MODULES
DC-TO-DC CONVERTER
CHASSIS

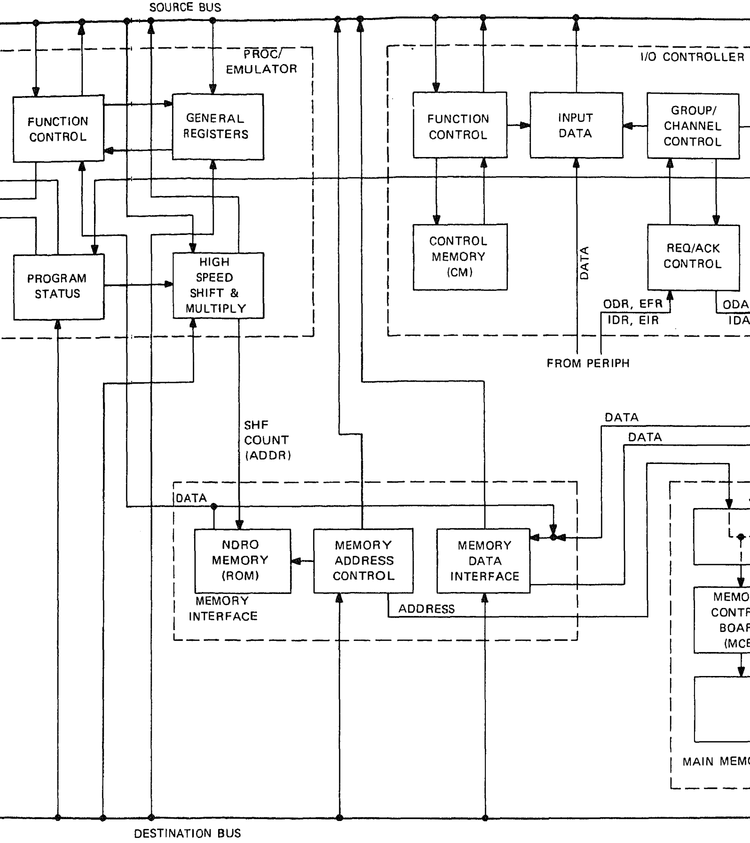

FEED-THROUGH FILTER CAPACITORS
0 VDC SWITCHING EGULATOR AND SCILLATOR
+90, +28, -5VDC RE CONVERT
0 VDC SWITCHING EGULATORS
POW TRA

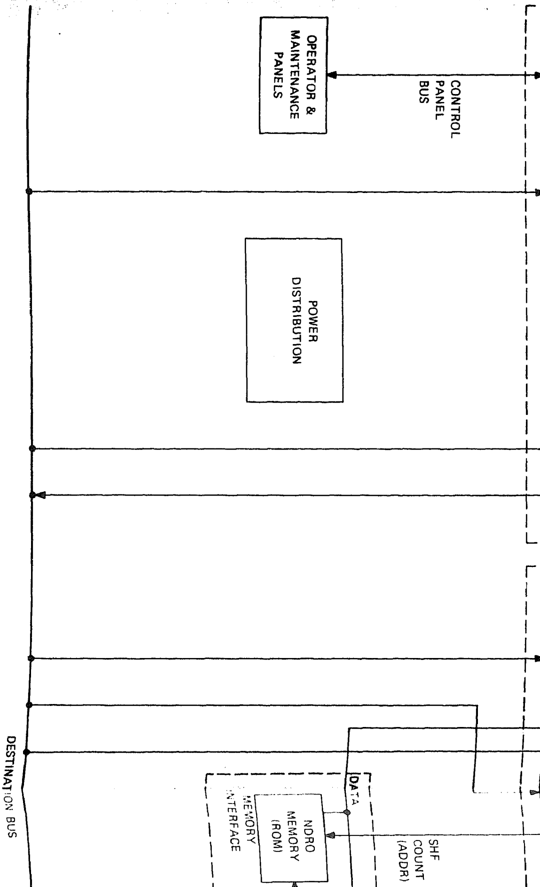
Synchronous Distributed Processor (SDP) and presented the interrelationship of the functional units, as well as a brief theory of their operation.

A brief discussion of the AN/UYK-7 computer was also presented. Although the use of this unit is not presently as widespread as the

rapid rate.

Again, a thorough un
material in this module is ess
to be presented in the mod
Subsystems presupposes thi
the information discussed in
modules is very important t
development.


SOURCE BUS
PROC/
EMULATOR
FUNCTION CONTROL
GENERAL REGISTERS
PROGRAM STATUS
HIGH SPEED SHIFT & MULTIPLY
I/O CONTROLLER
FUNCTION CONTROL
INPUT DATA
GROUP/ CHANNEL CONTROL
CONTROL MEMORY (CM)
DATA
REQ/ACK CONTROL
ODR, EFR
IDR, EIR
ODA
IDA
FROM PERIPH
SHF COUNT (ADDR)
DATA
DATA
DATA
NDRO MEMORY (ROM)
MEMORY ADDRESS CONTROL
MEMORY DATA INTERFACE
MEMORY INTERFACE
ADDRESS
MEMO
CONTR
BOAR
(MCE
MAIN MEMO
DESTINATION BUS


OPERATOR & MAINTENANCE PANELS
CONTROL PANEL BUS
POWER DISTRIBUTION
DESTINATION BUS
DATA
NDRO MEMORY (ROM)
MEMORY INTERFACE
SHF COUNT (ADDR)

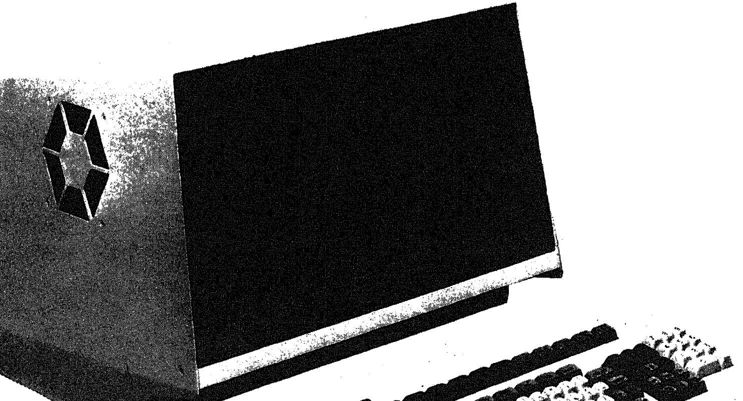
PART 3

PERIPHERAL EQUIPMENT

this module part we will examine some peri- l equipments that are commonly used ghout the Ocean Systems community. The ments discussed in this part, however, do not ent all the peripherals you may encounter ry facility. The theories and practices of the ments covered in this part will, with some fication, apply to other types of peripherals re likely to encounter. A comprehension of theories and practices will prove invaluable r efforts to effectively troubleshoot various systems and subsystems and return them operational status.

SUPER BEE COMPUTER TERMIN

The Super Bee Computer terminal (com called the Super Bee II, figure 3-1) is extensively throughout the Ocean Systems munity. It provides operator interface computer-based subsystem via a cathode-ra (CRT) display screen and keyboard. Althou



following discussion applies to the Super Bee II unit, the theories and general practices applicable to this unit can also be applied to other types of CRT computer terminals.

GENERAL DESCRIPTION

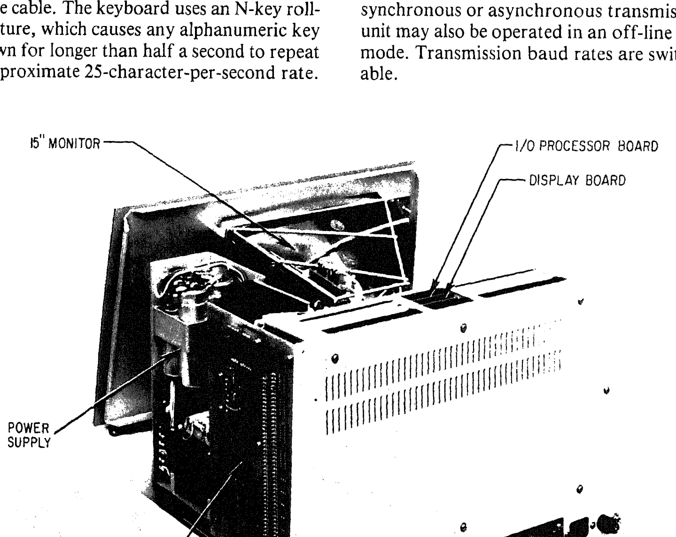
The Super Bee II computer terminal is a self-contained, operator-controlled, remote display terminal with a detachable keyboard. The receipt and transmission of data via this device are in serial format. The data exchange is variable in the range of 110 to 9600 baud. A 15-inch display monitor (measured diagonally) displays up to 25 lines of data, with 80 characters per line. Each character consists of a 5 × 7 dot matrix, and adjacent characters are separated by a two-dot space.

The keyboard is interfaced to the terminal via a flexible cable. The keyboard uses an N-key roll-over feature, which causes any alphanumeric key held down for longer than half a second to repeat at an approximate 25-character-per-second rate.

The Super Bee can be interfaced w
more external devices via rear panel c
(figure 3-2). The input/output an
connectors are wired parallel and will
with most American Standard Code for
tion Interchange (ASCII) printers. Pr
can be transmitted at a different baud
that of the terminal input/output and i
in the range of 110 to 9600 baud. A remo
monitor, which may be located up to
from the Super Bee, may be operated fro
connector via the rear panel.

COMMUNICATION CHARACTERISTICS

The computer terminal can be op
either a half-duplex or full-duplex m
synchronous or asynchronous transmis
unit may also be operated in an off-line
mode. Transmission baud rates are swit
able.



or Full Duplex

anel switch allows operation of the the half-duplex (HDX) or full-duplex . The RESET key (located on the ust be pressed following a change o FDX or vice versa. Full duplex ansmission and receipt of data at ne; half duplex allows either the or receipt of data, but not simul-

JPLEX.—During full-duplex oper- iver input of the terminal is enabled, the transmission of data with each ry. The computer receives and stores , at the same time, loops (echos) the the terminal for display. This opera- echoplexing.

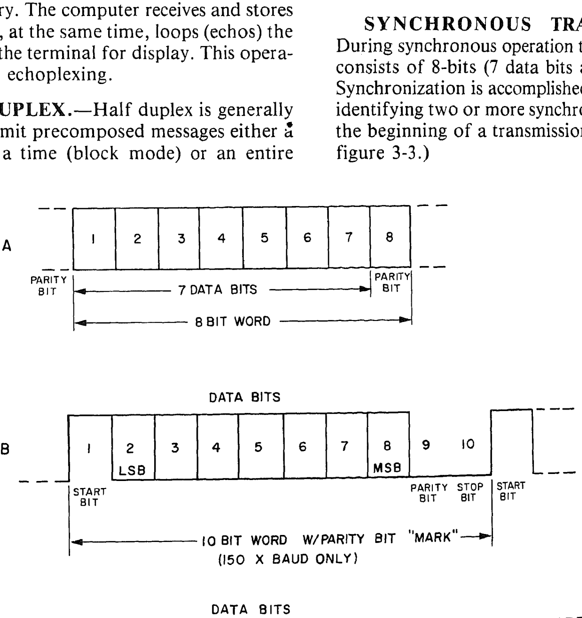
UPLEX.—Half duplex is generally mit precomposed messages either a a time (block mode) or an entire memory dump (2048, 8-bit words maximum) (page mode). During page or block mode data transmission the keyboard is disabled.

The half-duplex block mode transmission operation is used in most subsystems that use the Super Bee within the Ocean Systems community. This allows the operator to prepare and edit off-line data as a unit and then transmit the data.

Synchronous-Asynchronous Transmission

The terminal can transmit data in either the synchronous or asynchronous mode. A brief description of the word structure associated with these types of data transmission follows.

SYNCHRONOUS TRANSMISSION.— During synchronous operation the word structure consists of 8-bits (7 data bits and a parity bit). Synchronization is accomplished by receiving and identifying two or more synchronization codes at the beginning of a transmission. (See view A of figure 3-3.)



ASYNCHRONOUS TRANSMISSION.—The asynchronous word structure consists of a start bit, 7 data bits, a parity bit, and 1 or 2 stop bits. (One stop bit is used if the baud rate multiplier switch is set to the X150 position (view B of figure 3-3) and 2 stop bits when in the X110 position (view C of figure 3-3).

BAUD RATE SELECTION

The transmission rates of the terminals are switch selectable by controls located on the rear panel of the unit. The baud rate switch has seven positions: 1, 2, 4, 8, 16, 32, and 64. The baud rate multiplier switch has two positions: X110 and X150. Depending on the position of the multiplier switch, the selected baud rate is multiplied by either 110 or 150. Baud rates of 150, 300, 600, 1200, 2400, 4800, and 9600 are possible with a 10-bit-word operation (asynchronous and multiplier switch at X150). Rates of 110, 220, 440, 880, 1760, 3520, and 7040 are possible for an 11-bit-word operation (asynchronous and multiplier switch at X110).

DISPLAY ORGANIZATION

The display of the Super Bee computer terminal is organized on a page basis. Each page contains 25 lines with a maximum of 80 character positions in each line (2K characters can be displayed at any one time). If a line has less than 80 characters, the display will contain blanks or spaces to fill the line.

Certain data elements may have their video characteristics enhanced to alert operating personnel of certain alarm or status conditions. These include:

- Normal video display—Normal characters on a dark background.

- Normal video blinking—Consists of characters blinking alternately on and off.

- Reverse video—This is just the reverse of the normal display. Here, the background is

technique is known as efficien
number of memory locatio
However, if only 7 character
of 256 lines of 7 characters
(256 represents the maximun
the Super Bee). Of these
characters per line) only 25 c
any one time. The operat
controls on the keyboard to s
or down to bring any 25-line

It must be pointed out
characters per line are used
jump to nonexistent memory
contents of memory cannot
condition may result in loss
until power is removed and

When a clear operation
the CLEAR key on the keybo
was in memory is eradicated,
is filled with space codes,
positioned to the home posit
display screen). As the operat
new display characters repla
where indicated by the curso

The cursor is always displ
If the operator initiates any c
move it off the screen, the
matically scroll up or down to

MEMORY OVERWRITE

When data input has fille
locations, CURSOR RIGH
DOWN (keyboard) functions
prevents the cursor from m
end of memory (EOM). I
memory appears as the first
SCROLL UP, NEXT PAGE,
and CURSOR DOWN functi
that they do not move the
EOM. When the memory is
key), horizontal tab (HT),
data causes memory overwr
this occurs the data previousl

● Cursor is on line 25, between columns 0
nd 48 and a CURSOR DOWN function is
epeatedly attempted.

● Cursor is on line 25, column 48 and a CUR-
SOR RIGHT function is repeatedly attempted.

UNIT OPERATION

To become proficient in the maintenance
of the Super Bee computer terminal, you
must familiarize yourself with the
procedures involved with this uni
3-4 shows the physical layout of
board controls and indicators. F
with these controls and indicators
as the rear panel controls will allo
determine the operational status of
and to isolate casualties to a particul
circuit board or electronic assembly. F
shows the physical layout of the r

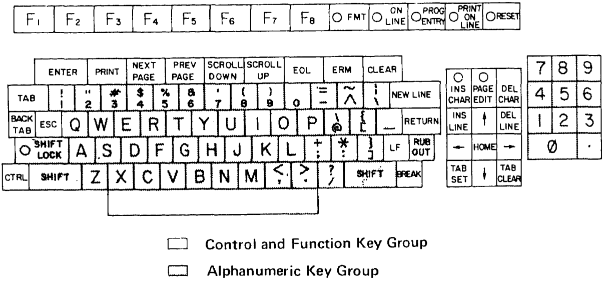


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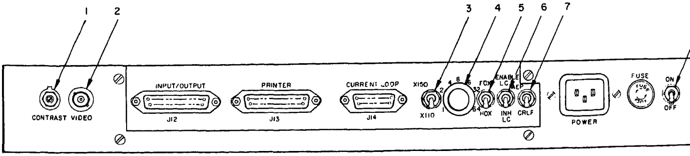
Figure 3-4.—Keyboard controls and indicators.



a. Rear Panel Controls - with Current Loop Adapter

Table 3-1.—Super Bee computer terminal rear panel controls

INDEX No.	CONTROL	FUNCTION
1	CONTRAST	Adjustment that sets contrast level of video on disp
2	VIDEO Output	Outputs composite video signal to remote monitor.
3	AUTO EFF PAGE-CRLF Switch	When set to AUTO EFF PAGE (auto efficient pagir the CR-LF code sequence generates a NEW LINE fu When set to CR-LF, the CR-LF code sequence is pe normally.
4	I/O Baud Rate Multiplier Switch	When set to 150, the selected baud rate is multiplie 150. When set to 110, the selected baud rate is mult by 110. Changes the length of the word depending whether the terminal is in synchronous or asynchro mode.
5	I/O Baud Rate Select Switch	Seven-position selector switch that selects basic rate 4, 8, 16, 32, and 64. Basic rate is multiplied by eith 150, determined by position of Multiplier Switch.
6	HDX-FDX Switch	Selects half-duplex (HDX) or full duplex (FDX) op conjunction with the RESET key. RESET key must depressed following selection of FDX or HDX befo terminal will make the change.
7	INH LC Switch	When set to INH LC (inhibit lower case), the alpha codes selected from the keyboard are stored in the and transmitted out on the I/O as upper case codes. case characters received by the I/O are displayed as case. When the switch is set to the Off position (up) keyboard generates all upper and lower case charact
8	Power ON-OFF Switch	Applies ac power to terminal.

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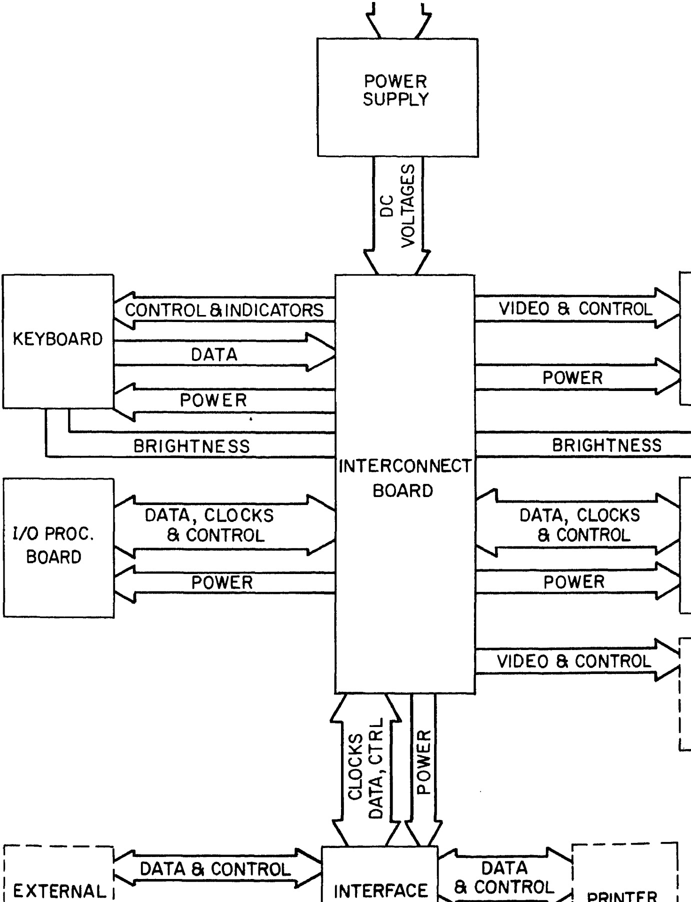
POWER SUPPLY
DC VOLTAGES
KEYBOARD
CONTROL & INDICATORS
DATA
POWER
BRIGHTNESS
INTERCONNECT BOARD
VIDEO & CONTROL
POWER
BRIGHTNESS
I/O PROC. BOARD
DATA, CLOCKS & CONTROL
POWER
DATA, CLOCKS & CONTROL
POWER
VIDEO & CONTROL
CLOCKS DATA, CTRL
POWER
EXTERNAL
DATA & CONTROL
INTERFACE
DATA & CONTROL
PRINTER

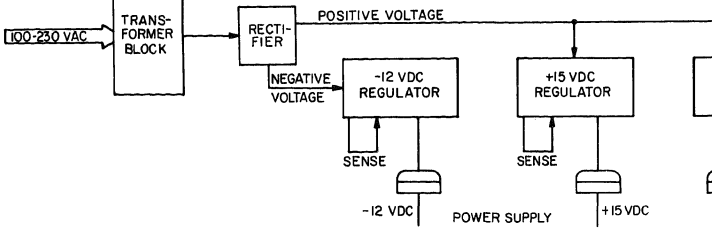

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Figure 3-7.—Power supply block diagram.

versions are available), input power can range from 100 to 220 V ac at 50 to 60 Hz. Figure 3-7 shows a power supply block diagram of the Super Bee. Most of the Super Bees you will encounter are configured for 117 V ac, single phase, 60 Hz.

Keyboard

The keyboard of the Super Bee is a manual input device that the operator uses to communicate with the terminal. The keyboard is similar to that of a standard teletypewriter but is expanded to include the capabilities of the Super Bee. The keyboard contains the key switches and supporting circuitry to generate the appropriate character and control codes. This unit also contains the video brightness control, various mode indicators, power indicator, and a set of eight special function keys. The keyboard is connected to the terminal by a flexible cable which is about 3 feet long. It is extremely important that the keyboard be attached to the terminal when power is applied. Without the brightness control in the circuit the monitor will power up to full intensity and possibly damage the CRT.

The keyboard is compatible with American National Standard Institute (ANSI) criteria. The characters are encoded into 8-bit codes (7 ASCII

A code chart for ASCII charac
in figure 3-8. Bits 1 through 4 a
side of the chart, and bits 5 throug
top. We will use the letter D as an e
ASCII coding method. After you
D on the chart, read the left co
lowest 4-bit sequence. If the least
(LSB) is placed in the rightmost
sequence will read 0100. Now, reac
the high-order 3-bit sequence. Th
100 (most significant bit (MSB
position). If these two sequences a
the ASCII code for D will read
capital letter Y is indicated by 101
the right).

As was shown in figure 3-4,
key functions are divided into t
follows:

- Control and function key
tains keys for all necessary move
cursor data, receive data, and
within the Super Bee II.

- Alphanumeric key group—
for generating all characters (numb
within the Super Bee II.

	CHARACTERS		CHARACTER					
BIT 765 4321	000	001	010	011	100	101	110	111
0000	NUL	DLE	SP	0	@	P	\	p
0001	SOH	DC1 ENTER	!	1	A	Q	a	q
0010	STX	DC2	″	2	B	R	b	r
0011	ETX	DC3	#	3	C	S	c	s
0100	EOT	DC4	$	4	D	T	d	t
0101	ENQ	NAK	%	5	E	U	e	u
0110	ACK OFF LINE	SYN	&	6	F	V	f	v
0111	BEL	ETB (XMIT)	'	7	G	W	g	w
1000	BS	CAN	(	8	H	X	h	x
1001	HT	EM	)	9	I	Y	i	y
1010	LF	SUB	*	:	J	Z	j	z
1011	VT	ESC	+	;	K	[	k	{
1100	FF	FS	,	<	L	\	l	¦
1101	CR	GS	—	=	M	]	m	}
1110	SO	RS	.	>	N	Λ	n	∽
1111	SI	US NEW LINE	/	?	O	—	o	RUB OUT

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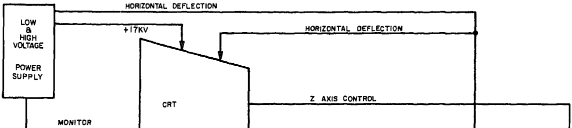
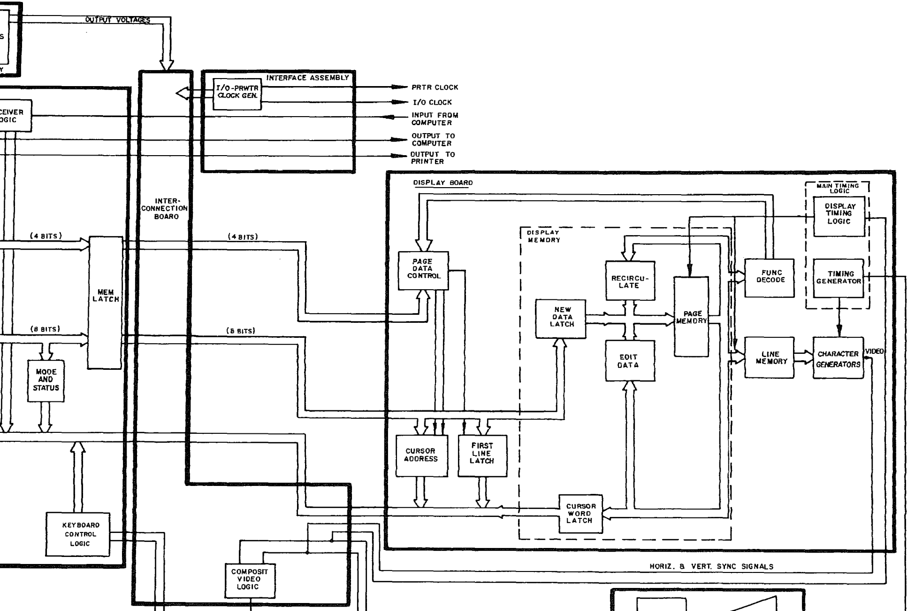
Figure 3-8.—ASCII code chart.




OUTPUT VOLTAGES
INTERFACE ASSEMBLY
I/O-PRWTR CLOCK GEN.
PRTR CLOCK
I/O CLOCK
INPUT FROM COMPUTER
OUTPUT TO COMPUTER
OUTPUT TO PRINTER
CEIVER
OGIC
INTER-CONNECTION BOARO
(4 BITS)
(8 BITS)
MEM LATCH
MODE AND STATUS
KEYBOARO CONTROL LOGIC
COMPOSIT VIDEO LOGIC
(4 BITS)
(8 BITS)
DISPLAY BOARD
PAGE DATA CONTROL
CURSOR ADDRESS
FIRST LINE LATCH
DISPLAY MEMORY
NEW DATA LATCH
RECIRCU-LATE
EDIT DATA
PAGE MEMORY
CURSOR WORD LATCH
FUNC DECODE
LINE MEMORY
MAIN TIMING LOGIC
DISPLAY TIMING LOGIC
TIMING GENERATOR
CHARACTER GENERATORS
VIDEO
HORIZ. & VERT. SYNC SIGNALS

. The control of brightness and contrast
tions is provided by external controls on the
board and back panel, respectively. The
itor is powered by + 15 V dc and CRT high
age from the low- and high-voltage power
ly. The high voltage power supply levels
vary depending on various configurations
alled.

lay Board

The display board (figure 3-10) contains
e data control, cursor control logic, display
nory, line memory, character generation
c, and main timing logic.

The page data control decodes four control
from the micro-processor to determine how
eight data bits from the I/O processor board
be used. These data bits may be used by the
or control logic to change the cursor loca-
or determine which line of memory will be
layed as the first line of the display. These
bits may also represent a character that is
e stored in display memory.

The cursor control logic consists of the
or address logic which controls the cursor
tion and the first line latch which is used to
rmine which line of memory will be displayed
e first line of the display.

All information that is displayed on the
en of the terminal is stored in display
nory. The display memory consists of the
data latch, page memory, recirculate logic,
data latch, and the cursor word latch. The
data latch is controlled by page data control
the cursor address logic. Page memory is
posed of two banks of shift registers, each
aining 1024 × 8 bit locations for storage of
acters. This gives a total of 2048 × 8 bits of
age. The recirculate logic allows the character
out from page memory to be recirculated to
nput of page memory for storage. The recir-
te logic is inhibited when a new character is
remaining data in page memory is recircu
through the edit data latch vice the recirc
logic. As each character is recirculated thr
the edit data latch it is delayed by one
pulse. This continues for all remaining da
page memory until all data has been recircul
To update the page memory when the
reaches the cursor location, the new data
is enabled so as to output data onto the
memory input bus. The new data enter
memory and replaces the data lost by inhib
the recirculate latch (the recirculate lat
inhibited because of the write operation—
Data Latch enabled and Recirculate I
disabled). Therefore, a character in memor
be overwritten with a new character. A
cursor time (refers to the position of the c
in memory and the data above this pos
during a read cycle) other data in page me
is loaded into the cursor word latch to be
by the microprocessor. The cursor word
works with the microprocessor to allow chara
read out of page memory to be transmitt
the computer. This provides the microproc
with the ability to read data from page mem

The line memory is an 80 × 7 shift re
memory which stores up to 80 characters.
line memory is loaded from page memory
outputs data to the video generation logi
the actual display of the characters or
display screen.

The timing generator generates the ti
signals that provide for digital vertical
horizontal sync on the CRT. The timing gene
also specifies the amount of time allotted to
dot, character, scan, and line of the display
main timing chain contains logic for genera
timing, and controlling the display of the term
including cursor control, display and char
generation, line memory, page memory,
edit functions.

I/O Processor Board

The microprocessor consists of an Intel 8008-1 MOS chip. This component (called an 8-bit parallel central processor unit) includes an instruction register, memory, arithmetic-logic unit (ALU), and input/output buffers. The microprocessor uses instructions and data stored in the program memory (7 ROM chips each containing 256 × 8 bit words for a total of 1729 × 8 bit words) to control the operation of the terminal.

The microprocessor loads 8 bits of data from the output bus and 4 bits of data from the control bus into the memory latch. The memory latch retains this data until it is synchronized with the page memory. The page data control decodes the 4-bit control bus sequence and determines how the 8-bit output bus sequence is to be used. The microprocessor can read from the cursor address and first line latch back into memory latch. This helps define the cursor character number and the cursor line number, which ultimately determine the position of the cursor.

The mode and status latch contains information that defines the operating mode of the terminal and the status of various signals. The status latch indicates the availability of conditions within the hardware, such as receiver done, transmitter busy, and KPD (keyboard) done.

The transmit logic serializes data from the output bus and transmits the data to an external device, such as a printer. This data may be either a 10- or an 11-bit asynchronous word or an 8-bit synchronous word and may be transmitted at baud rates of up to 9600 baud. The receive logic receives serial RS-232 data from the data source and converts the data into 8-bit parallel words. The data is then applied to the microprocessor for processing under direction of the program memory. Serial data may be received synchronously or asynchronously up to 9600 baud. The receive logic indicates to the microprocessor that data is available for the input bus. The micro-

terminal subassemblies. It serv
distribution for power and fac
change of signals among the
also contains a speaker (for th
an optional elapsed time indic

Interface Assembly

The interface assembly (fi
faces the I/O processor board
data source and a printer.
signals that facilitate the I/C
also generated here.

The Interface Assembly
subassemblies: connector boar
board-A2 (not shown in figure

Connector board-A1 is a di
of all standard RS-232 data an
between the I/O board and
device printer.

Switchboard-A2 contains a
switch that, in conjunction wi
switch (figure 3-5), allows
different baud rates from 110 t
tion of the multiplier switch
either a 10- or an 11-bit wo
Other switch options include:

FDX/HDX—Full duplex/h

AEF/CRLF—Auto efficient
return line feed

ENABLE LC/INH LC—E
acter/inhibit lower character.

In addition, TTL XMIT (tra
logic transmit) clock and prin
are generated in switchboard-
are variable by selecting certai

TERMINET 1200 PRINTER

s when the following alarm conditions occur (remains on
has been corrected):

r out
ot on forms tractor model)
of paper or end of magnetic tape in "Write" mode if in
: Send-Receive (ASR) configuration.
ter.

ndicator lights, the following occurs:

nds
reak is automatically transmitted to alert the other end
e)

onditions that do not light the ALARM indicator but sound
n Interrupt or Break to be transmitted, and turn off the

: 300 Printers only)
nter.
ed.

n is corrected, LOCAL or ON LINE must be pressed to

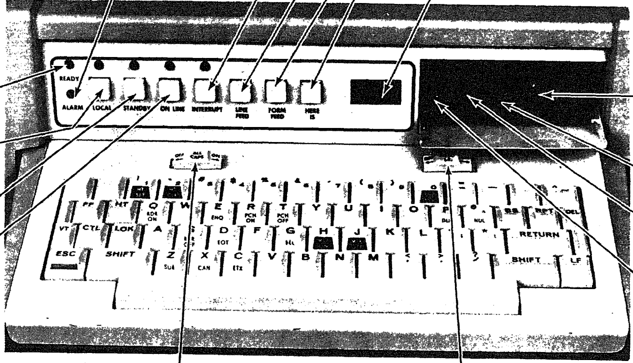
INTERRUPT - See INTERRUPT CONDITION TABLE 3-1.

LINE FEED - Will cause paper to feed one line each time it is pressed and quickly released. When pressed and held, paper will continue to line feed incrementally.

FORM FEED - When pressed, causes paper to feed continuously to the beginning of the next new form.

HERE IS - triggers answerback code if the Printer has the answerback option.

PRINT POSITION INDICATOR - Shows position of next character to be printed.



SPACE -

- Set on "1", single line-space.
- Set on "2", double line-space. (Only 1 line-feed character sent externally for each generated LF.)

RATE - Selects the Printing, Transmitting and Receiving speed of the Printer and optional tape equipment.

INHIBIT -

- PRINT position, inhibits printing and paper punching from local source.
- OFF position, printing is normal.
- TRANS position, inhibits transmission of data; incoming data not affected.

TRANSPARENCY - Allows the Printer to process (receive or transmit) codes other than ASCII but inhibits printing.

ALL CAPS - When placed in the ON position, all alphabetic printing caused by the keyboard only will be upper case.

AUTO L.F. - When in the ON position, the paper is advanced automatically when the RETURN key is pressed. (Has no effect on incoming data.)

the theories and practices discussed in the next paragraphs can be applied to other types of printer units.

Specifications

The TermiNet 1200 is available in three models as follows:

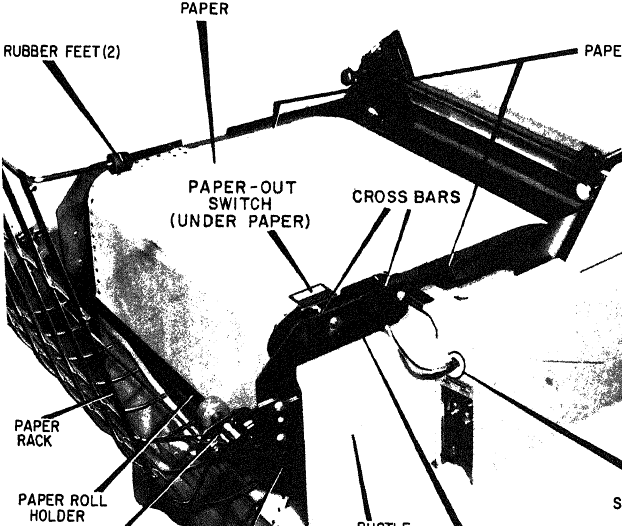
- Keyboard Send Receive (KSR)
- Send Receive (SR); no keyboard installed
- Receive Only (RO); no keyboard installed.

The printer conforms to the Electronic Industries Association (EIA) Standard RS-232C

receive data at the followi

- 110
- 115
- 200
- 300
- 600
- 1200

Standard speeds of 10, per second (CPS) are ope Optional speeds of 15, 20 specified when the equipme



At 10 CPS, the unit code (word length) is 11
(1 bit for start, 7 bits for intelligence, 1 bit
parity, and 2 stop bits). At 15, 20, 30, 60, and
CPS, the unit code is the same except that
one stop bit is used (10 bits). The start bit
lways a O. The stop bit is always a 1. The
ter can transmit and/or receive all 128 ASCII
racters (94 printable characters and 32 special/
trol characters. Two other characters, SP
DEL, are not printed but are sent).

Horizontal character spacing is 10 pitch (10
racters per inch). The printer is available with
er 80 or 120 print positions per line. A digital
t-emitting diode (LED) display print position
cator is mounted on the control panel of the
ter indicating the next column in which print-
is to occur. A printer-controlled end-of-line
ning alarm (beep) sounds eight print positions
ore the end of the print line (as preselected).
The end-of-line alarm also sounds when the
print position is reached. Both of these alarms
active for locally generated data (data entered

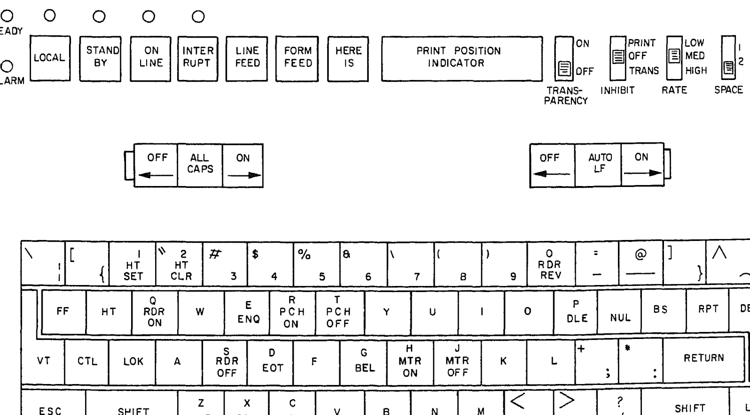
switch (1 or 2). The printer is equipped wi
adjustable width paper tractor mechanism (f
3-12) for use with continuous feed, edge-pun
paper. The printer can accommodate p
ranging in width from 3 inches to 12.85 in
Multipart forms of up to 6 parts may be
(maximum form thickness is .25 inch). An
of form sensor activates an alarm when the p
supply has 16 inches or less remaining.

Controls and Indicators

The following discussion is intende
familiarize you with the controls and indic
used to operate the TermiNet 1200 printer
effectively maintain this equipment, you
understand its operation.

CONTROL PANEL.—Figure 3-11 show
location of the switches and indicators o
control panel and explains their basic funct

KEYBOARD.—The keyboard (figure
used with the TermiNet 1200 is a stan



can generate special codes on the keyboard. The ESC and its associated keys are shaded. Most of the control keys are identified on their front edge. The keys are electronically interlocked so that the simultaneous generation of two ASCII codes is not possible. An audible tone is generated each time a key is pressed (does not apply to the SHIFT, CTL, LOK, and RPT keys).

The keys normally used for routine operation of the printer are as follows:

- FF (form feed)—Causes the paper to advance to a predetermined line.

- HT (horizontal tab)—Moves the print position horizontally to a predetermined place.

- BS (backspace)—Moves the print position one position to the left without printing a character.

- RPT (repeat)—Causes any other pressed character to repeat at the rate of 5 characters per second.

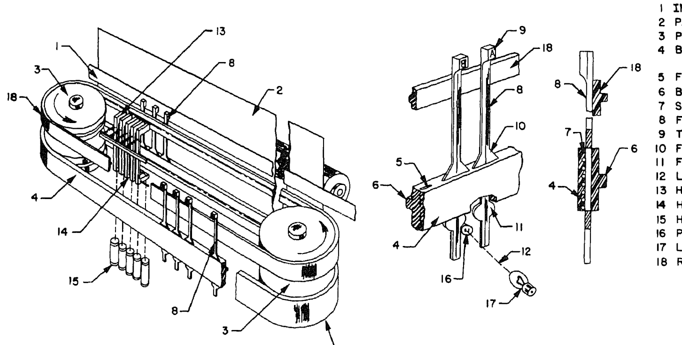
- RETURN with the AU
feed). If the AUTO LF switch i
tion, pressing the RETURN ke
position to cycle to the left mar
LF switch is in the ON positic
RETURN key causes the print
to position No. 1 and causes a l

- SHIFT and LOK (sh
used in conjunction with ot
uppercase characters to be pr
mitted. The LOK key mecha
SHIFT key in the activated st
SHIFT key on the left side of
deactivate the locked state.)

- SPACE BAR—Moves
one position to the right.

- VT (vertical Tab) (optic
paper to advance to a predete

- ESC (Escape)—This
produce an escape code and is
combination with other special



w. Once the escape code is activated, the character is inhibited from printing.

1. HT SET (horizontal tab set)—Sets a at the position indicated by the PRINT ITION INDICATOR. Any number of tabs be set on a print line.

2. HT CLEAR (horizontal tab clear)—rs all tabs.

3. MTR ON (motor on)—Activates the iNet electric motor.

4. MTR OFF (motor off)—Deactivates motor.

5. RDR REV (reader reverse)—Causes rsal of an optional tape recorder.

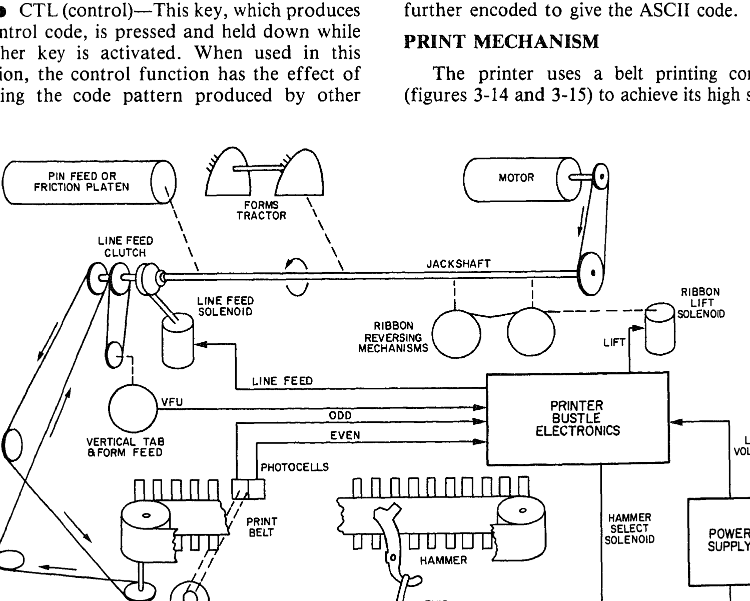
- CTL (control)—This key, which produces ntrol code, is pressed and held down while her key is activated. When used in this ion, the control function has the effect of ing the code pattern produced by other keys. The function of the control key comb tions depends, to a large degree, on the inst tion of certain options. We will not discus specific functions of the control key combina in this module. You should refer to the appr ate TermiNet 1200 operators manual for det information on the use of the control cod

KEY ENCODING

Key encoding occurs when a key is pre which causes electromagnetic coupling of a signal line and two sense lines. These line routed through the magnetic core that is ciated with the key. The sense lines gener preliminary row and column code, whic further encoded to give the ASCII code.

PRINT MECHANISM

The printer uses a belt printing co (figures 3-14 and 3-15) to achieve its high s



(font) has a type character or symbol embossed on its upper end. There are two complete sets of 96 characters on the belt. Printing occurs when a hammer is activated ("fired"), which strikes the print finger to be printed. The print finger is then driven against the ribbon, paper, and a platen (roller much like a typewriter platen), which accomplishes the print operation. The hammer and print finger then rebound back to their original position. There is a hammer for each of the 120 print positions.

For belt type printing to work, precise synchronization must be achieved. The printer compares the positions of the print fingers in front of the hammers. The hammer is activated (fired) when the "called for" print finger is in the correct position. Timing and synchronization a result, the controlling logic is continuously informed of the position of the print fingers with respect to the hammer. The position of each finger (character) is relative to the position of several wide index fingers, which are detected by the photocell light beam. Two such wide index fingers are installed on the print belt to separate the two sets of 96 characters. Index fingers are wider at the bottom than at the top. They serve as a reference point to trigger an electronic counting circuit used for activating the hammer circuits.

ELECTRONIC LOGIC MODULE

The main electronic module (commonly called the "bustle") is mounted at the rear of the

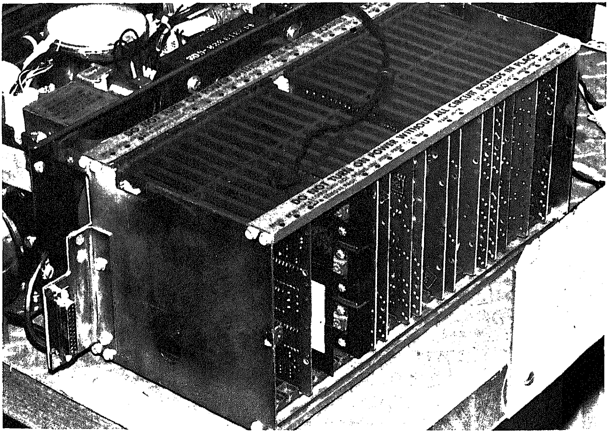


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Figure 3-16.—Bustle.

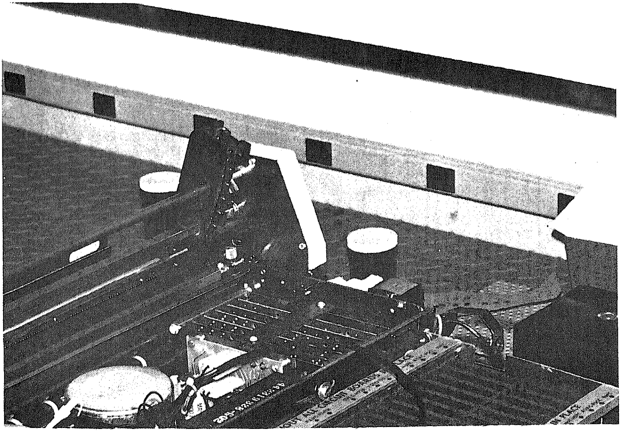
are designed for interchangeability to keep maintenance and service to a minimum. The logic circuits are designed so that most of the basic functions and options are on one printed circuit board and can be replaced or added as needed. Horizontal tabulating and parity checking are examples of options that can be added at user discretion. The functions of certain printed circuit boards can be changed by the positioning of "jumper" connectors.

In addition to the bustle mounted at the rear of the printer, which contains the "main" printed circuit boards, there is a minibustle (figure 3-17). The minibustle is located at the mid-portion of the printer on the left side (as viewed from the top front). The minibustle contains

Functional Block Diagram

Refer to figure 3-18 as you review the discussion presented in this section. From the keyboard, the 7-bit parallel ASCII code is sent to the Parallel-to-Serial Converter (PSCC/9) printed circuit board (PCB). The PSCC/9 PCB manipulates the received data to convert it from a parallel to a serial format. This serial data, along with a parity check bit, is then sent to an interface Data Set Control (DATC/2) PCB.

The DATC/2 is an RS-232 interface. It receives serial data from the PSCC/9 PCB, performs voltage and power level changes on received data, and, when called upon to do so, transmits the data to a computer or other terminal. The DATC/2 PCB also receives the



182.198.4

Figure 3-17.—Minibustle.

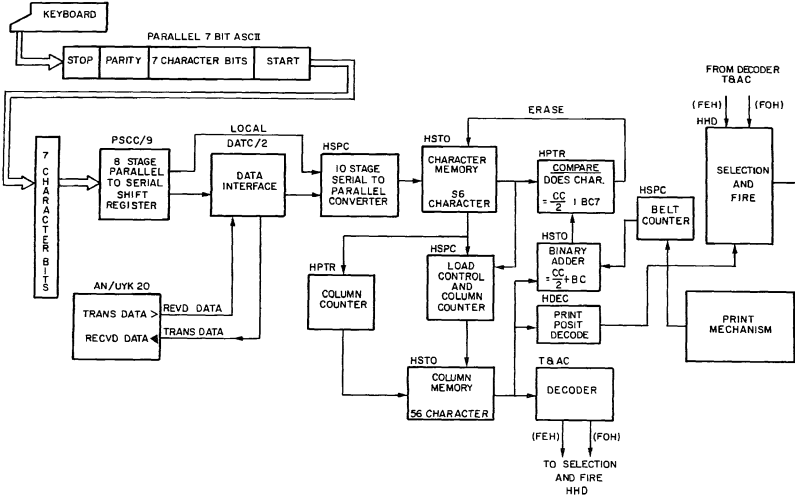


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Figure 3-18.—TermiNet functional block diagram.

HSPC board.

The HSPC PCB receives data from both the PSCC/9 and the DATC/2 PCB. Data from the PSCC/9 board generally represents data entered at the keyboard when the unit is operating in the LOCAL mode (processed locally but not transmitted). The HSPC receives data in a serial format and converts the data to a parallel format. It also decodes the received data to recognize the following functions:

- Escape codes
- Control codes
- Character to be printed.

The circuitry for interrupt detection, as well as that which provides a controlled inhibit of the print function (INHIBIT switch is in the PRINT position or the TRANSPARENCY switch is on), is contained on this board. The HSPC also controls the belt counting process, which keeps track of the fingers (fonts) passing the photocell. This process keeps an accurate column count and generates an erase signal to the HSTO PCB to erase nonprint characters immediately and printable characters after they are printed. The HSPC outputs data to the HSTO PCB (memory storage).

The HSTO PCB can store up to 56 characters of information in memory. Upon receipt of the applicable signals from the HSPC PCB character, information is erased (from memory) once a character has been selected for printing. In this regard, the HSTO keeps track of the next print column to be used and sends this information to the HDEC serial decoder PCB. The HSTO also sends a "fire" signal to the T&AC PCB, which activates a print hammer at the appropriate time. The HDEC (serial decoder) PCB, after viewing the column information from the HSTO PCB, decodes and amplifies the information and then sends it to the HHD PCB. The T&AC PCB (timing and alarm), which has received the "fire" signal from the HSTO PCB, gates the incoming signal and amplifies it to produce either a fire even hammer (FEH) or a fire odd hammer (FOH) response.

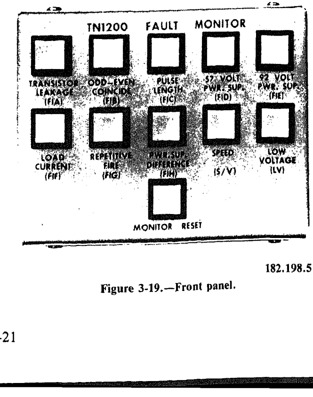
The T&AC PCB also generates the signals (500 Hz and 1000 Hz) for various beep tones used in printer operation, along with the circuits the HHD (hammer head controller) PCB. The HPTR (printer control) PCB can be configured to accommodate 120-column printers. The column number to be printed is transmitted to the HSTO PCB for processing. In addition, the HPTR loads the column memory and facilitates such other items such as the line-feed logic, ribbon-feed logic, load logic, and 8-state up/down binary counter.

The HHD PCB contains a silicone-controlled rectifier (SCR) for each hammer position. The FEH and FOH signals from the T&AC PCB, along with the "called for" column position information from the HDEC PCB, are processed causing signal outputs to the electromechanical print mechanism.

The previous discussion was designed to give you a brief overview of the theory of operation of the TermiNet. It does not encompass all PCBs or electromechanical items used with this printer. More specific information can be obtained from the manufacturers technical manuals for the TermiNet 1200.

Troubleshooting

Fault localization on the TermiNet 1200 printer is facilitated by the use of the fault monitor. The front panel of this device is shown in figure 3-19. This device is a small



182.198.5

Figure 3-19.—Front panel.

has 11 pushbutton indicator switches. The interfacing plug is connected to the HHD PCB of the printer, via a connector on the front-left corner of the board (figure 3-20). When the fault monitor is connected to the printer and power is applied, it will indicate certain faults in the printer (appropriate push-button switch will illuminate).

Normal troubleshooting procedures involve the use of general purpose electronic test equipment (GPETE), such as multimeters, oscilloscopes, and so forth. Card (PCB) swapping with known good spares can also be done; however, caution must be exercised to prevent damage to good cards.

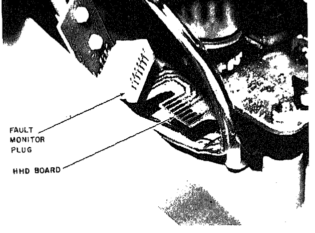


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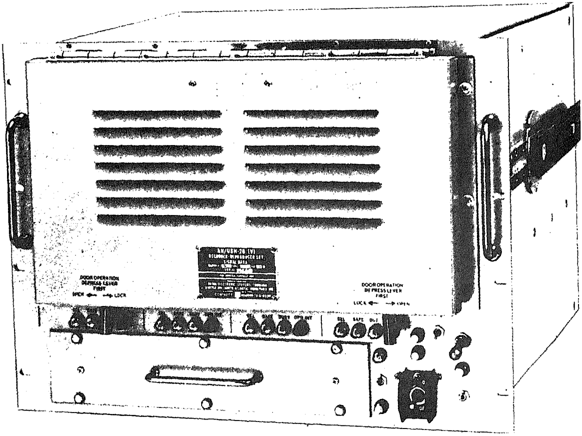
Figure 3-20.—Printer connection.



182.200

Figure 3-21.—AN/USH-26(V) Recorder-Reproducer Set, Signal Data.

RECORDER-REPRODUCER

The AN/USH-26 (figure 3-21) is a cartridge ype of magnetic tape recorder-reproducer that s used to interface with a general-purpose digital computer, such as the AN/UYK-20. The

depending upon the installation of certain options. The AN/USH-26 consists of a single unit, which can accommodate up to four individual tape drives (figure 3-22). The unit responds to computer-generated commands of read and write operations, tape position, reset function, and status responses. It has a maintenance panel

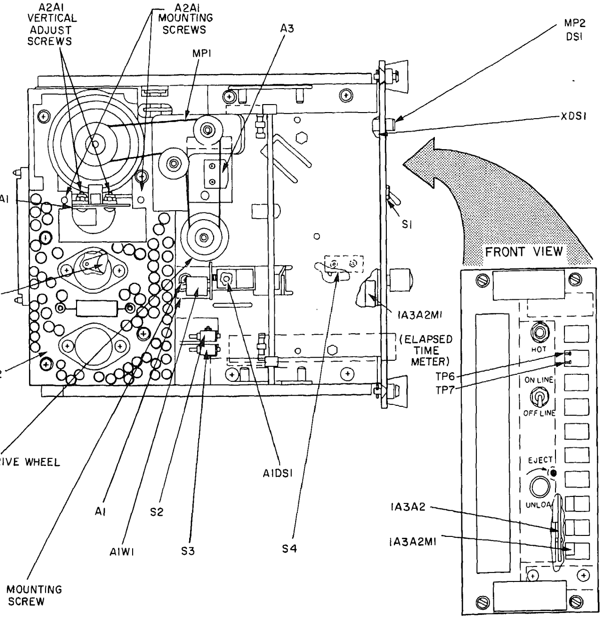


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Figure 3-22.—Tape drive asembly.

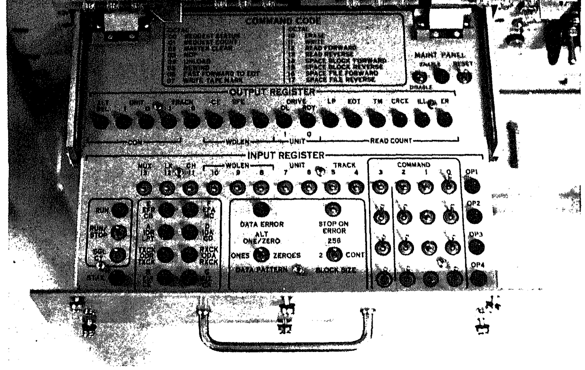

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Figure 3-23.—Maintenance panel assembly (1A9).

(figure 3-23), which permits manual control for maintenance purposes.

The front of the unit includes a hinged front cover, which contains an air filter. The basic controls and indicators used in routine operation of the unit are also mounted on the front panel. The maintenance panel, which is mounted on slides, is accessible from this area.

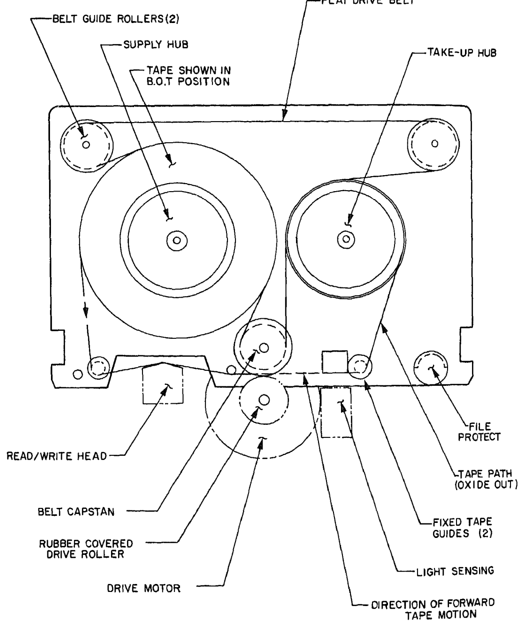
With the hinged front cover in the raised position, the tape drive units are accessible, along with the control and indicators used for routine operation.

Magnetic Tape Cartridge

The magnetic tape cartridge consists of 1/4-inch-wide tape that is wound on two hubs with an internal drive belt to transport the tape between the hubs (figure 3-24). The tape has four data tracks (figure 3-25), and each track is independent of the other. Phase encoding is the method used to record on the data tracks. Each data bit requires a reversal of flux polarity in a given direction for a logic 1 and in the opposite direction for a logic 0. The normal recording density is 1600 bits per inch.

The tape has several holes punched into it to facilitate tape positioning and movement (figure 3-26). These holes are commonly called markers, and their purpose and position are as follows:

- Beginning of tape (BOT) marker—The BOT marker consists of three sets of two holes. The innermost set of holes is used to identify the storage position of the cartridge. In the storage position all of the permissible recording area is wound on the supply hub and protected by at least one layer of tape. Cartridges removed



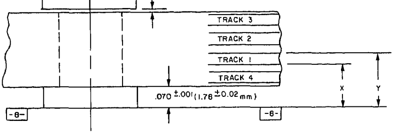
182.201

Figure 3-24.—Cartridge diagram.

from the tape drive are usually automatically rewound to the storage position before removal. The additional sets of holes are used to ensure reliability of detection.

- Load point (LP) Marker—This marker consists of one hole punched in the tape to indicate the beginning of the permissible recording area in the forward direction.

- Usable recording area—An area 6 inches after load point to $24 + 3 - 0$ inches ($609.6 + 76.2 - 0$ mm) after the early warning (EW) marker and is 4 tracks in width.



TRACK DIMENSIONS TO CARTRIDGE REFERENCE

TRACK	INCHES				MILLIMETERS			
	DIMENSION X		DIMENSION Y		DIMENSION X		DIMENSION Y	
	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
1	.146	.130	.194	.178	3.71	3.30	4.93	4.52
2	.210	.194	.258	.242	5.33	4.93	6.55	6.15
3	.274	.258	.322	.306	6.96	6.55	8.18	7.77
4	.082	.066	.130	.114	2.08	1.68	3.30	2.90

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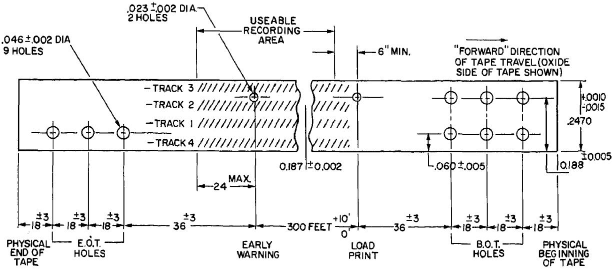
Figure 3-25.—Tape guide and track dimensions.



TOLERANCE AS NOTED
DIMENSIONS IN INCHES

182.201.2

Figure 3-26.—Tape position holes and recording format.

f the permissible recording area in the forward irection. The recording must halt before the nd of tape (EOT) marker is sensed.

● End of tape (EOT) marker—The EOT arkers consist of three single holes along a ngle line. The first hole indicates that the ermissible recording area has been exceeded. he additional holes are used to ensure reliability f detection.

PERATION

The AN/USH-26 requires minimal operator nterface during automatic operation. The N/USH-26 responds to computer commands nd data words supplied by the computer. When command word is received, the AN/USH-26 nternal logic circuits interpret and accomplish he required operation. Command and data words re transmitted via a parallel or serial interface count words to the host computer. The operator is responsible for the off-line operations of the equipment. These operations include power-up, tape cartridge loading and unloading, and power-down. Through effective use of the maintenance panel, the operator can aid in isolating system casualties.

AN/USH-26 Controls and Indicators

To become an effective maintenance technician, you must understand the functions of the controls and indicators mounted on the AN/USH-26. A thorough knowledge of the following information will enhance your ability to isolate system casualties and return the recorder-reproducer to an operational status.

FRONT PANEL CONTROLS AND INDICATORS.—Figure 3-27 and table 3-2 illustrate

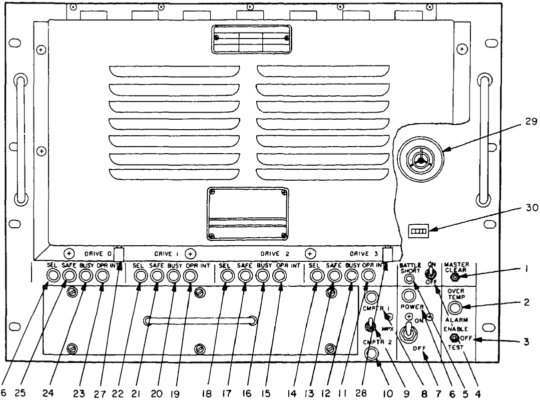


Figure 3-27.—Front panel controls and indicators.

INDEX NUMBER	CONTROL/INDICATOR	FUNCTION
1	MASTER CLEAR two position return-to-neutral toggle switch	When activated, resets the entire AN/USH-26(V) (Performs the same function as the Master Clear command).
2	OVERTEMP indicator (incandescent with red lens)	When lit, indicates the ambient temperature within the AN/USH-26(V) exceeds 140° F (60° C).
3	ALARM ENABLE/OFF/TEST three position toggle switch	When set to ENABLE, enables the audible alarm function. When set to OFF, disables the audible alarm function. When set to TEST, causes the audible alarm to sound and the OVERTEMP and Tape Drive Assembly HOT indicators to light.
4	BATTLE SHORT ON/OFF two position toggle switch	When set to ON, disables the overtemperature shutdown function. BATTLE SHORT indicator is lit. When set to OFF, enables the overtemperature shutdown function.
5	BATTLE SHORT indicator (LED with red lens)	When lit, indicates the BATTLE SHORT ON/OFF switch is in the ON position.
6	POWER indicator (incandescent with green lens)	When lit, indicates primary power is applied to the AN/USH-26(V).
7	POWER ON/OFF two position circuit breaker	When set to ON, enables primary power to the AN/USH-26(V). When set to OFF, disables primary power to the AN/USH-26(V).

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INDEX NUMBER	CONTROL/INDICATOR	FUNCTION
8	CMPTR1 indicator (LED with clear lens)	When lit, indicates the AN/USH-26(V) is operating with computer 1. Flashes during multiplex operation.
9	CMPTR1/MPX/CMPTR2 three position toggle switch	When set to CMPTR1, allows AN/USH-26(V) to operate with computer 1. When set to MPX, allows AN/USH-26(V) to operate with computer 1 or computer 2, or with both computers 1 and 2 (multiplex). When set to CMPTR2, allows AN/USH-26(V) to operate with computer 2.
10	CMPTR2 indicator (LED with clear lens)	When lit, indicates the AN/USH-26(V) is operating with computer 2. Flashes during multiplex operation.
11	DRIVE 3 OPR INT indicator (LED with red lens)	When lit, operator intervention is required for Tape Drive Assembly 3.
12	DRIVE 3 BUSY indicator (LED with clear lens)	When lit, Tape Drive Assembly 3 is performing a motion command.
13	DRIVE 3 SAFE indicator (LED with clear lens)	When lit, indicates cartridge in Tape Drive Assembly 3 is file protected.
14	DRIVE 3 SEL indicator (LED with clear lens)	When lit, indicates that Tape Drive Assembly 3 has been selected.
15	DRIVE 2 OPR INT indicator (LED with red lens)	When lit, operator intervention is required for Tape Drive Assembly 2.
16	DRIVE 2 BUSY indicator (LED with clear lens)	When lit, Tape Drive Assembly 2 is performing a motion command.

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INDEX NUMBER	CONTROL/INDICATOR	FUNCTION
17	DRIVE 2 SAFE indicator (LED with clear lens)	When lit, indicates cartridge in Tape Drive Assembly 2 is file protected.
18	DRIVE 2 SEL indicator (LED with clear lens)	When lit, indicates that Tape Drive Assembly 2 has been selected.
19	DRIVE 1 OPR INT indicator (LED with red lens)	When lit, operator intervention is required for Tape Drive Assembly 1.
20	DRIVE 1 BUSY indicator (LED with clear lens)	When lit, Tape Drive Assembly 1 is performing a motion command.
21	DRIVE 1 SAFE indicator (LED with clear lens)	When lit, indicates cartridge in Tape Drive Assembly 1 is file protected.
22	DRIVE 1 SEL indicator (LED with clear lens)	When lit, indicates that Tape Drive Assembly 1 has been selected.
23	DRIVE 0 OPR INT indicator (LED with red lens)	When lit, operator intervention is required for Tape Drive Assembly 0.
24	DRIVE 0 BUSY indicator (LED with clear lens)	When lit, Tape Drive Assembly 0 is performing a motion command.
25	DRIVE 0 SAFE indicator (LED with clear lens)	When lit, indicates cartridge in Tape Drive Assembly 0 is file protected.
26	DRIVE 0 SEL indicator (LED with clear lens)	When lit, indicates that Tape Drive Assembly 0 has been selected.
27	Latch for outer door	Move to left in conjunction with Index 28 to release latch and access tape drives.

INDEX NUMBER	CONTROL/INDICATOR	FUNCTION
28	Latch for outer door	Move to right in conjunction with Index 27 to release latch and access tape drives.
29	Audible Alarm	Alarm sounds if the ALARM ENABLE/OFF/TEST switch is in the ENABLE position or if the safe operating temperatures have been exceeded.
30	Time meter - 4 digit, 0000 to 9999	Records accumulated hours that primary power has been applied.

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d briefly describe the controls and indicators ounted on the front panel of the AN/USH-26. ith the exception of the alarm horn and time eter, access to all controls and indicators is ained with the front cover in the closed posi- on. (This does not include controls and dicators on the individual tape drive units.)

TAPE DRIVE ASSEMBLY CONTROLS ND INDICATORS.—Figure 3-28 and table 3 illustrate and briefly describe the individual pe drive controls and indicators. These controls d indicators are the same for each tape drive ounted in the AN/USH-26. The front panel of e unit must be in the raised position to gain ccess to the controls and indicators.

UNCTIONAL DESCRIPTION

As we mentioned earlier, the AN/USH-26 is magnetic tape handling system designed to terface with a general-purpose digital com- uter. The unit is functionally divided into six verall areas (foldout 3-1, at the end of this apter): driver/receiver, interface circuits, rmatter circuits, drive circuits, maintenance anel circuits, and power circuits.

river/Receiver Circuits

The driver/receiver circuits serve the purpose f level conversion and provide signal coupling to and from the host computer. Parallel and serial interfaces can be provided by these circuits.

Parallel Interface

There are three types of parallel interfaces available for use in the AN/USH-26:

- Driver/Receiver A—Used to interface the AN/USH-26 with computers requiring NTDS Slow (– 15 V) (MIL-STD-1397 TYPE A) parallel data transfers.

- Driver/Receiver B—Used to meet the requirements of NTDS Fast (–3.5 V) (MIL-STD-1397 TYPE B) parallel data transfers.

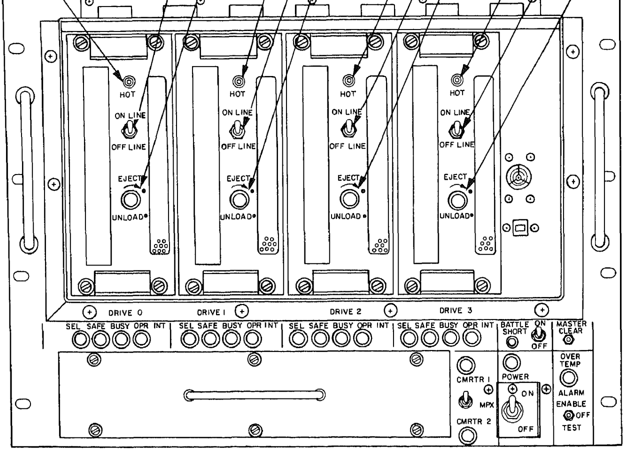
- Driver/Receiver C—Used to meet the requirements of ANEW (+3.5 V) (MIL-STD-1397 TYPE C) parallel data transfers.

Serial Interface

There are two types of serial driver/receiver circuits for use in the AN/USH-26:

- Driver/Receiver MIL-STD-188C—Used to meet the requirements of MIS-STD-188C synchronous data transfers.

- Driver/Receiver RS-232C—Used for RS-232C serial synchronous data transfers.



182.202.2

Figure 3-28.—Tape drive assembly controls and indicators.

Regardless of the type of circuit used, the overall purpose of the driver/receiver circuits is to accept control and data inputs from the computer (receiver) and to supply response and data outputs to the computer (driver).

Interface Circuits

There are three interfaces that can be used with the AN/USH-26. Serial interface is used when a serial format is called for and one computer is used. Parallel interface can be either parallel or multiplex parallel. Parallel interface is used when a parallel format is called for and only one computer is used. Multiplex parallel, on the other hand, is used when two computers are used with a parallel format.

The interfaces provide command word decoding and storage, provide status words and responses to the computer (via the drivers), and supply formatter control and data signals to the formatter logic.

Formatter Circuits

There are three formatter cards used in the AN/USH-26: Formatter A, Formatter B, and Formatter C.

- Formatter A—The primary function of this formatter is to interpret and decode

INDEX NUMBER	CONTROL/INDICATOR	FUNCTION
1	Drive 0 HOT indicator (incandescent with red lens)	When lit, indicates Tape Drive Assembly 0 temperature exceeds 165° F (74° C). It is also lit when the ALARM ENABLE/OFF/TEST switch is set to TEST.
2	ON LINE/OFF LINE two position toggle switch	When set to ON LINE, places Tape Drive Assembly 0 in operational condition. When set to OFF LINE, places Tape Drive Assembly 0 in non-operational condition.
3	EJECT/UNLOAD rotary switch	Enables operator to unload or mechanically eject the tape cartridge from Tape Drive Assembly 0.
4	Drive 1 HOT indicator (incandescent with red lens)	When lit, indicates Tape Drive Assembly 1 temperature exceeds 165° F (74° C). It is also lit when the ALARM ENABLE/OFF/TEST switch is set to TEST.
5	ON LINE/OFF LINE two position toggle switch	When set to ON LINE, places Tape Drive Assembly 1 in operational condition. When set to OFF LINE, places Tape Drive Assembly 1 in non-operational condition.
6	EJECT/UNLOAD rotary switch	Enables operator to unload or mechanically eject the tape cartridge from Tape Drive Assembly 1.

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INDEX NUMBER	CONTROL/INDICATOR	FUNCTION
7	Drive 2 HOT indicator (incandescent with red lens)	When lit, indicates Tape Drive Assembly 2 temperature exceeds 165° F (74° C). It is also lit when the ALARM ENABLE/OFF/TEST switch is set to TEST.
8	ON LINE/OFF LINE two position toggle switch	When set to ON LINE, places Tape Drive Assembly 2 in operational condition. When set to OFF LINE, places Tape Drive Assembly 2 in non-operational condition.
9	EJECT/UNLOAD rotary switch	Enables operator to unload or mechanically eject the tape cartridge from Tape Drive Assembly 2.
10	Drive 3 HOT indicator (incandescent with red lens)	When lit, indicates Tape Drive Assembly 3 temperature exceeds 165° F (74° C). It is also lit when the ALARM ENABLE/OFF/TEST switch is set to TEST.
11	ON LINE/OFF LINE two position toggle switch	When set to ON LINE, places Tape Drive Assembly 3 in operational condition. When set to OFF LINE, places Tape Drive Assembly 3 in non-operational condition.
12	EJECT/UNLOAD rotary switch	Enables operator to unload or mechanically eject the tape cartridge from Tape Drive Assembly 3.

182.202.3

starting and stopping. Additional functions pertain to multiplex operation, word length, and determining when valid read data is present.

- Formatter B—The main functions of this formatter are to convert serial output data during a read operation to a parallel format and parallel input data to a serial format for writing.

- Formatter C—Formatter C is an extension of formatter B and is used to accommodate longer word lengths and to incorporate the system clock.

Tape Drive Circuits

As we discussed earlier, the AN/USH-26 can incorporate up to four modular tape drive assemblies. Each tape drive assembly consists of a tape drive chassis assembly and a transport interface card. Associated with each tape drive assembly is a control card and a servo/data board. The control card and servo/data board are mounted on the chassis of the AN/USH-26 unit and are not part of the tape drive assembly. All tape drive control and status signals enter and leave the Control Card. Tape drive and track selection signals determine where reading and writing is to be performed. Tape drive commands are logically combined with internal status signals to control tape motion. Precise control of tape motion is done by electronically comparing actual tape motion (represented by an electrical signal) with a reference signal in the servo/data board.

Monitoring of the tape motion is accomplished by an optical tachometer and a transport interface card, both of which are mounted on the tape drive chassis assembly. Tape marks (magnetic areas recorded on the tape) are sensed by the tape head. Tape position is sensed by the tape mark sensor assembly, which provides tape position information. Read data is transferred

Maintenance Control Circuits

There are two types of maintenance control circuits used in the AN/USH-26, depending on whether parallel or serial interfaces are installed. Each maintenance control circuit consists of a maintenance panel assembly (figure 3-23) and an associated maintenance control card. The maintenance control circuits allow the operator to simulate and observe the results of a computer command. These circuits are used primarily as a tool in troubleshooting and fault isolation.

Power Circuits

There are six optional power supplies available for use in the AN/USH-26, only one of which can be installed in any one unit.

COMPUNETICS ASYNCHRONOUS CHANNEL MULTIPLEXER (ACM) MODEL 27010

For a man-machine interface (MMI) device (such as the TermiNet 1200 or Super Bee computer terminal) to communicate with a computer, access must be provided to the input/output channels of the computer. The AN/UYK-20 computer, for example, has 16 I/O channels. Other computer channel configurations may vary, depending upon the type of machine in use. The connection of one channel of a computer to only one MMI device is often inefficient and greatly reduces the capability of the computer, both from a processing and hardware standpoint. Often, there are more than 16 MMI devices in an operational environment which, if you were to use one channel with one MMI device, would require several computers. To eliminate this limitation, you can use the Asynchronous Channel Multiplexer (ACM) Model 27010, which is manufactured by

182.20

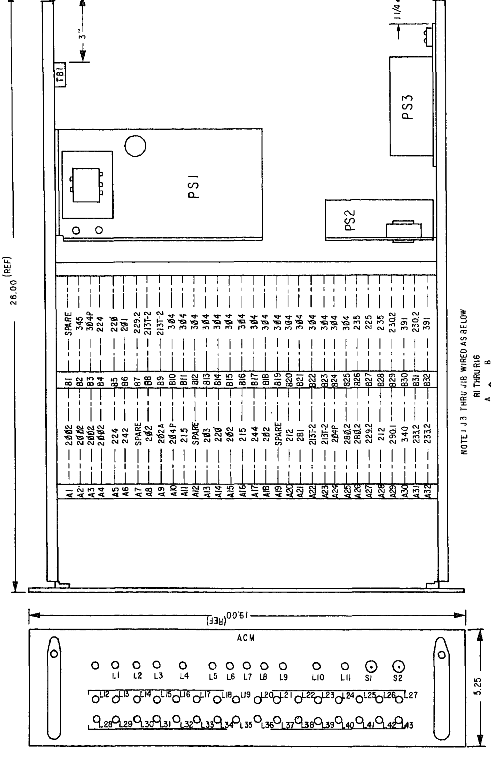


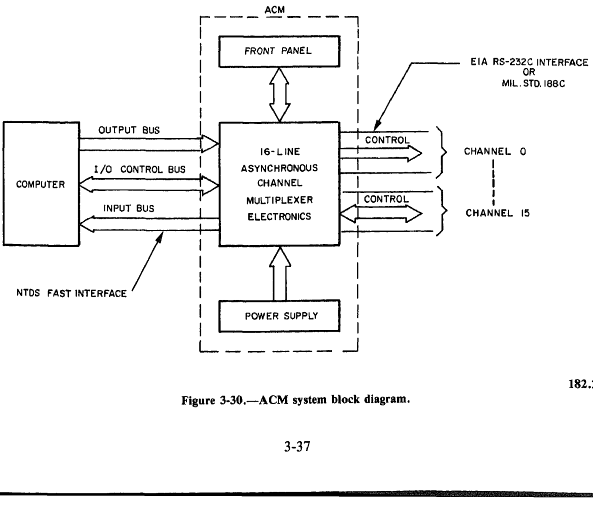
Figure 3-29.—Model 27010 ACM, chassis top view.

The switching operation is accomplished by time division multiplexing, which is used for manipulating both transmitted and received data. The ACM also operates in a full duplex mode. The result of the multiplexing (sometimes called MUX) greatly expands the number of devices with which a computer may communicate (only one channel is used for up to 16 devices). It also greatly reduces the I/O processing time required of the computer. (Once again, a channel that carries 16 devices can be processed.) This reduction in processing time enables the computer to accomplish its primary mission of data processing more effectively. Figure 3-30 is a block diagram representation of a typical ACM installation.

A channel scanner is used in the ACM to accomplish the switching operation. The channel scanner "looks at" each of the 16 channels of

storage areas (buffers) are required for this operation. One area, called the transmit memory, holds and distributes data from the computer to the proper device. Transmit memory for each channel can accommodate up to 127 8-bit words of information. The combined memory capacity of the 16 transmit memories is therefore on the order of 2K (8 bit) words. A second storage area, called the first in-first out (FIFO) memory, collects data from the MMI devices for forwarding to the computer. (The FIFO memory can accommodate up to 4K 8-bit words of information.)

To better understand the function of an ACM, you may think of it as having a channel scanner that acts as an electronic switch, a FIFO memory that serves as a data collector (for forwarding to the computer), and a transmit memory that serves as a data collector (for distribution to the MMI devices).



182.203.1

Figure 3-30.—ACM system block diagram.

INDICATOR	DESCRIPTION
RECEIVE 0-15	Sixteen indicators, one for each channel; indicate receiver line activity by monitoring the corresponding line's received data signal.
TRANSMIT 0-15	Sixteen indicators, one for each channel; indicate transmitter line activity by monitoring the corresponding line's transmit data signal.
COMPUTER	
EIR	External interrupt request. When illuminated, indicates the asserted state of EIR, which generates an interrupt request to the computer.
IDR	Input data request. The ACM asserts this signal to the computer when the ACM has data it wishes to transfer to the computer.
IDA	Input data acknowledge. This signal originates at the computer and indicates to the ACM, that the computer has accepted the data placed on the computer input bus by the ACM.
ODR	Output data request. This signal originates at the ACM. When asserted indicates to the computer that the ACM requires data from the computer.
ODA	Output data acknowledge. This signal originates at the computer. It indicates to the ACM, that the computer output bus contains valid information. ODA clocks the data into the ACM.
FIFO	
FULL	When illuminated it indicates the 4K FIFO memory is filled with 4096 characters. Under normal operation such a condition should never occur.
EMPTY	When illuminated it indicates that no characters are present in the 4K FIFO memory. Will illuminate only upon becoming empty following a FIFO FULL condition.

POWER	
+5	When illuminated indicates the +5 volt power supply is energized.
-5	When illuminated indicates the -5 volt power supply is energized.
+12	When illuminated indicates the +12 volt power supply is energized.
-12	When illuminated indicates the -12 volt power supply is energized.
SCAN	This signal indicates that the channel scanner counter is sequencing.
LT	Lamp test. When depressed illuminates all indicators for operational verification.
MC	Master clear. When depressed places the ACM into the idle state and resets all flag bits and registers.
POWER	Applies power to the ACM.

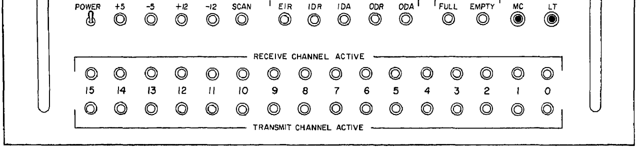
182.203.2

OPERATION

During normal system operation, no operator intervention is required. The ACM operates under complete control of the host computer software. Indicators are available for performance monitoring and as troubleshooting aids during maintenance procedures. Table 3-4 lists all controls and indicators located on the front panel of the ACM, along with a brief description of their function. Figure 3-31 illustrates the switch and indicator layout of the front chassis. Figure 3-32 illustrates the rear panel of the ACM from which connections of up to 16 MMI devices can be made. Also contained on the rear panel are jacks for interfacing the unit to a computer (J1 & J2) and a power jack and circuit breaker.

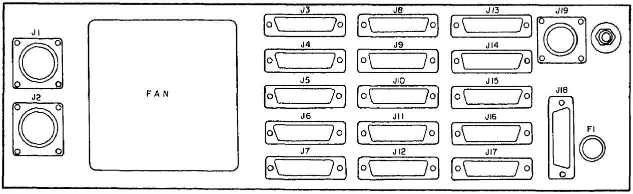
TRANSMIT MODE

The computer, when transmitting data to the ACM, loads a message of up to 127 × 8-bit characters into an internal buffer within the ACM. One such buffer is available for each of the 16 serial channels. This results in a memory capacity on the order of 2K × 8-bit characters (equates to the transmit memory mentioned earlier). The specific buffer area to be loaded is indicated by the high-order byte of the first 16-bit word transferred to the ACM. This high-order byte is called the terminal address (TA).



182.203.3

Figure 3-31.—Model 27010 ACM, chassis front view.



182.203.4

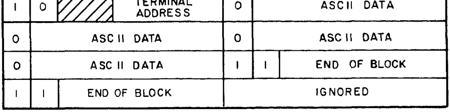
Figure 3-32.—Model 27010 ACM, rear panel components.

Data transmission from the ACM to the MMI device begins when the memory loading sequence is completed. This completion is sensed by recognition of the end-of-block (EOB) bits in a character, which is transmitted from the computer to the ACM. The message length is therefore terminated by the EOB bits. Any character containing the EOB sequence cannot be a valid data type of character. The maximum message length is 126 data characters plus the EOB character (127 characters total).

Data transmission from the ACM to a MMI device is in a binary (1s and 0s) serial format. The appropriate data block (127 characters) is selected from the transmit memory of the ACM. The block is then loaded character by character into the appropriate Universal Asynchronous Receiver/Transmitter (UART) card for transmission to the MMI device. After the message is completely transmitted, an interrupt signal is generated by the ACM to the computer that informs the computer of the message status.

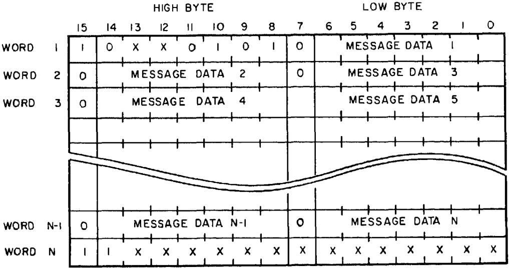
Figure 3-33 illustrates all possible variations for the 16-bit computer output word. With bit 15 reset (0), the ACM is informed that bits 08 to 14 contain an ASCII data character. With bit 7 reset (0), the ACM is informed of the same situation for bits 00 to 06. Data can therefore appear in either or both of the upper and lower bytes of the 16-bit word.

To initiate data transfer from the computer, a terminal address (TA) must be sent to the ACM. This TA must be contained in the high byte (bits 08 to 15) of the transmitted 16-bit



182.203.5

Figure 3-33.—Computer output word formats.



182.203.6

Figure 3-34.—Typical ACM message word formats.

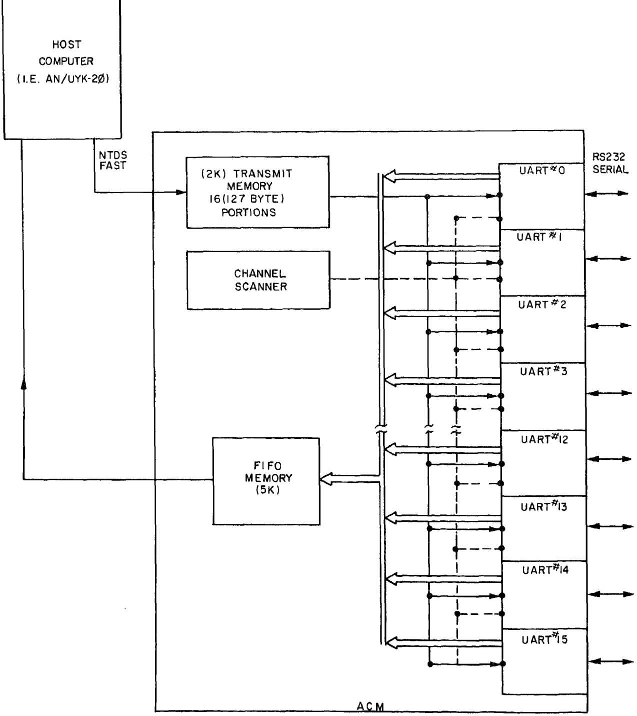
word. The low byte (00 to 07) of the first 16-bit word should never contain a TA. The low byte may contain an ASCII data character, which would be the first character of the message. With bit 15 set (1) and 14 reset (0), the byte is a TA and the address data will be in bits 8 to 11.

The EOB condition will be indicated if both high-order bits are set within a byte. When an EOB condition is encountered, the ACM ignores the remaining bits within the byte. The EOB sequence can appear in either the upper or lower byte. The ACM interprets all information as message data that is framed by the TA and EOB bits.

Figure 3-34 illustrates typical ACM message word· formats. This message is transmitted to ACM channel 5 as indicated by the state of bits 8 to 11 of word 1. Message data follows the TA sequence with the first character of the message being contained in bit positions 00 to 06 of word 1. Word N contains the EOB flag, which terminates the message.

RECEIVE MODE

Receive data originates at each of the MMI devices and is transmitted to the ACM via RS-232C/MILSTD 188C (MILSTD 188C with 304-2 type UART only). The UART cards of the



182.204

Figure 3-35.—Functional block diagram asynchronous channel multiplexer.

independently of the others. The outputs of the UARTs are loaded into the FIFO memory. (The FIFO memory has a 4K × 8-bit capacity.) The channel scanner sequences through each UART and loads the FIFO memory if the UART has a valid receive character available. Each character loaded into the FIFO memory, if originating from a different UART than the preceding character, is preceded by a TA indicating the channel from which the data character originated.

Circuitry operating independently of the UART/FIFO transfer reads data from the FIFO memory and transfers it to the computer via the NTDS Fast channel. This transfer sequence (FIFO memory to computer) is initiated when at least one valid data character is present in the FIFO memory.

All possible word formats transmitted to the computer by the ACM are shown in figure 3-36. Data received by the computer must be identified with its channel number to be meaningful to the computer program. As we discussed previously, this is accomplished by the use of the TA. The TA must be in the high-order byte (08 to 15) of the first 16 bit message word as transferred to the ACM (transmitted data). The TA can be in either the upper or lower byte for data input to the computer. Figure 3-36 contains two different TAs. With bit 15 set (1) and 14 reset (0), the TA condition is indicated. The same situation can apply to bits 07 and 06. All data following the occurrence of a TA is associated with the indicated channel until the next occurrence of a TA.

The computer can also be informed to ignore the low-order byte of a received word. This is done by setting bits 07 and 06 (1s).

Figure 3-37 shows some typical words transferred to the computer by the ACM. In this

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	▨	▨	TERMINAL ADDRESS				0	ASCII DATA						
0	ASCII DATA							0	ASCII DATA						
0	ASCII DATA							1	0	▨	▨	TERMINAL ADDRESS			
0	ASCII DATA							1	1	NO CHARACTER					

Figure 3-36.—Computer input word formats. **182.203.7**

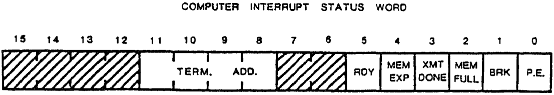
HIGH BYTE								LOW BYTE							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	▨	▨	1	0	0	1	0	CHANNEL 9 DATA						
1	0	▨	▨	0	1	1	1	0	CHANNEL 7 DATA						
0	CHANNEL 7 DATA							1	1	▨	▨	▨	▨	▨	▨
1	0	▨	▨	1	0	0	0	0	CHANNEL 8 DATA						
0	CHANNEL 8 DATA							1	0	▨	▨	0	0	1	1
0	CHANNEL 3 DATA							1	1	▨	▨	▨	▨	▨	▨

Figure 3-37.—Typical ACM receive message word formats. **182.203.8**

character associated with channel 9 in the low byte.

Bits 15 and 14 of word 2 define the high byte to contain another TA (channel 7) along

Word 3 contains a zero in bit 15 indicating that bits 08 to 14 contain still another data bit associated with channel 7. This is because no new TAs were defined since the TA for channel 7 was initiated. Note that word 3 has only one



BITS	DESCRIPTION
00	PARITY ERROR - THE ACM HAS DETECTED A PARITY ERROR IN THE RECEIVED DATA.
01	BREAK KEY - THE BREAK KEY WAS DEPRESSED AT THE TRANSMITTING TERMINAL (INCLUDES FRAME ERROR POSSIBILITY)
*02	MEMORY FULL - INDICATES THE FIFO MEMORY BUFFER IS FULL.
03	TRANSMIT DONE - INDICATES THE ACM HAS COMPLETED TRANSMISSION OF A MESSAGE.
*04	MEMORY EMPTY - INDICATES THE FIFO MEMORY BUFFER IS EMPTY.
05	NOT READY - INDICATES THE ACM ABORTED MESSAGE TRANSMISSION BECAUSE OF A TERMINAL-NOT-READY CONDITION. NOTE: WHEN BIT 05-1. BIT 03 WILL ALSO BE SET.
06-07	(NOT USED)
06-11	TERMINAL ADDRESS - INDICATES TO WHICH CHANNEL STATUS BITS 0, 1, 3, and 5 APPLY.

* THESE TWO CONDITIONS ARE NOT ASSOCIATED WITH A PARTICULAR CHANNEL.

182.203.9

Figure 3-38.—Computer interrupt status word.

Word 4 contains a TA of 8 and associated ta character in the low byte and another in the gh byte of word 5.

Word 5 also contains a TA of 3 in the low te with the associated data in the high byte of ɔrd 6.

TERRUPT

The status of the ACM is communicated to ɛ computer via the interrupt mechanism. An errupt normally occurs at the end of a message .nsmission, which has the effect of indicating 'transmit done'' to the computer. Each of the llowing conditions will also cause the interrupt ndition to occur:

- Parity error during receive
- Pressing a "break" key at one of the MMI terminals
- Transmit done
- Terminal (MMI) not ready
- FIFO memory full
- FIFO memory empty.

The interrupt status word (figure 3-38) is .nsferred over the same lines as the computer ɔut data. Since other types of data cannot cupy the line (bus) at the same time as an errupt status word, some form of priority ıst be established. In the ACM an interrupt ndition has priority over FIFO memory data .nsfers. The interrupt status word also contains ɛ terminal address of the channel initiating ɛ interrupt sequence if interrupt is channel pendent. FIFO Full and FIFO Empty are n-channel-dependent interrupts.

INPUT PROCESSOR UNIT (IPU 1-1)

The IPU 1-1 is used for formatting analog ta for processing by a computer-based system. such, you will often encounter this device thin the Ocean Systems community. A mprehension of the operation of this unit will ɔve invaluable because it is an integral part of ɛ signal path of a number of subsystems.

rack-mounted, digital frequency band analyzer. It can accept analog inputs from 80 beams of analog acoustic data and output 32 6-Hz bands of digitized acoustic data. The center frequency and beam selection for the 32 bands are computer program selectable. The unit uses complex bandshifting techniques to produce data for the output bands. Any of the 80 inputs can be selected for processing.

The processing capability of the IPU 1-1 can be doubled from 32 to 64 channels by adding external memory capabilities.

The construction of the IPU 1-1 is modular in design and is comprised of 25 circuit card assemblies (CCAs). These include:

- Ten anti-aliasing filter CCAs. The anti-aliasing filters remove undesirable frequency components from a data stream prior to further processing by the IPU.
- One beam selector and analog-to-digital converter CCA.
- Four arithmetic unit CCAs.
- One optional RAM expansion CCA.
- One sine/cosine generator CCA.
- One test CCA.
- One master clock CCA.
- One timer control No. 1 CCA.
- One timer control No. 2 CCA.
- One NTDS interface control CCA.
- One NTDS interface register CCA.
- Two NTDS interface driver/receiver CCAs.

Each of the CCAs is slide-guide mounted and can be easily removed from the front of the unit. Interconnections between the CCAs are made via a wire wrap "mother board."

As an aid in troubleshooting, each CCA has 45 color-coded test points along the front edge of the card.

The front panel of the unit contains various status indicators and a BNC connector for testing purposes. The rear panel (figure 3-40) contains a

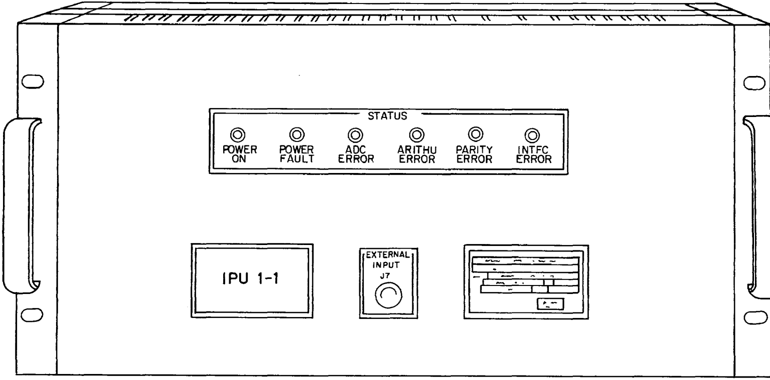


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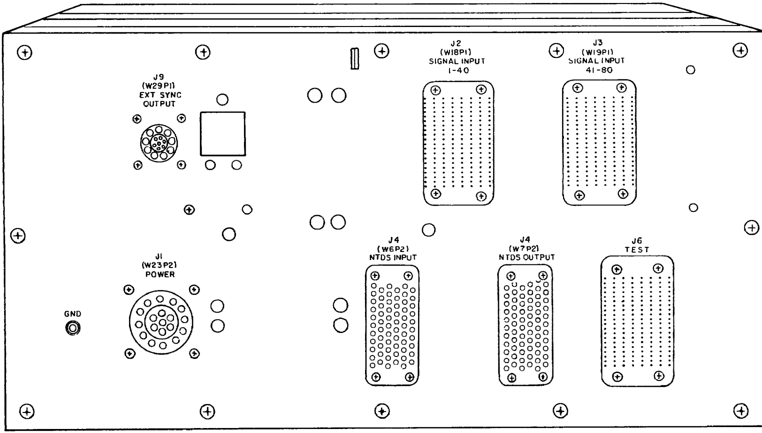
Figure 3-39.—IPU 1-1 front panel.



182.205.1

Figure 3-40.—IPU 1-1 rear panel.

Connector	Designation	
POWER ON Indicator	DS1	A green LED, lit when the primary power is applied to the IPU 1-1 by switching the POWER OFF/ON switch to ON.
POWER FAULT Indicator	DS2	A red LED, lit whenever a voltage out of tolerance condition has been detected in the primary power.
ADC ERROR Indicator	DS3	A red LED, lit when a fault has been detected in the Analog to Digital Converter Circuits.
ARITHU ERROR Indicator	DS4	A red LED, lit when a fault has been detected in the Arithmetic Processing.
PARITY ERROR Indicator	DS5	A red LED, lit when a parity error has been detected in the read-write memory.
INFC ERROR Indicator	DS6	A red LED, lit when a time-out fault has been detected in the Interface Circuits.
EXTERNAL INPUT Connector	J7	A BNC connector used to input an analog test signal (Input No. 81).

Table 3-6.—Function of connectors, IPU 1-1 rear panel

Connector	Reference Designation	Function
POWER Connector	J1	A 19-pin connector used to input the necessary power for the IPU 1-1.
SIGNAL INPUT Connector	J2	A 104-pin connector used to input 40 differential analog signals (1-40) into the IPU 1-1.
SIGNAL INPUT Connector	J3	A 104-pin connector used to input 40 differential analog signals (41-80) into the IPU 1-1.
NTDS INPUT Connector	J4	A 75-pin connector used to output 16 input data lines and 4 input control lines from the IPU 1-1 to the controlling computer.
NTDS OUTPUT Connector	J5	A 75-pin connector used to input 16 output data lines and 2 output control lines into the IPU 1-1 from the controlling computer.
TEST Connector	J6	A 104-pin connector used to provide access to IPU 1-1 timing signals and data lines for a special IPU 1-1 test equipment.
EXT SYNC OUTPUT Connector	J9	A 19-pin connector used to provide access to 6 differential lines and sync signal which are controlled by the connected computer.

OWER

The IPU 1-1 obtains its dc voltage requirements from a PSU-26 (Model 1, 2, or 3) power pply unit. The dc voltage levels are as follows:

- +15 V
- −15 V
- +5 V

ONTROLS AND INDICATORS

During normal on line operation, the IPU 1-1 quires little or no operator intervention. Hower, a comprehension of the controls, indicators, id connectors of the unit is necessary to ensure oper unit operation and to effectively isolate iit casualties. Table 3-5 describes the functions the front panel indicators and BNC connector. able 3-6 describes the functions of the rear anel connectors. When studying tables 3-5 and 6, you may find it necessary to refer to gures 3-40 and 3-41 to familiarize yourself with ie locations of the controls, indicators, and onnectors of the IPU 1-1.

UNCTIONAL DESCRIPTION

In the following discussion we will describe ie functions of the various types of CCAs used the IPU 1-1. The functional interrelationships nong these circuit cards are illustrated in figure 41.

ntialiasing Filter CCA

Each antialiasing CCA can process up to ght inputs. The input circuitry consists of the ollowing items:

- Differential receiver—This item provides nominal common mode rejection of 60 dB and gain of one-half dB.
- 5-Pole, low pass, active filter—Provides n attenuation of greater than 48 dB at and

conversion) and if not removed could produce false results during the A to D conversion process.

Beam Selector and A to D Converter CCA

The purpose of the beam selector and A to D converter CCA is to select a specific analog input from each of the 32 (64 with expanded memory installed) processing channels, time multiplex them, and convert them to digital form. This CCA consists of the following items:

- Analog multiplexers for formatting data prior to the A to D conversion process.
- A to D converters for converting the time multiplexer analog input to a digital format.
- Registers for storing the required beam number and digital output.

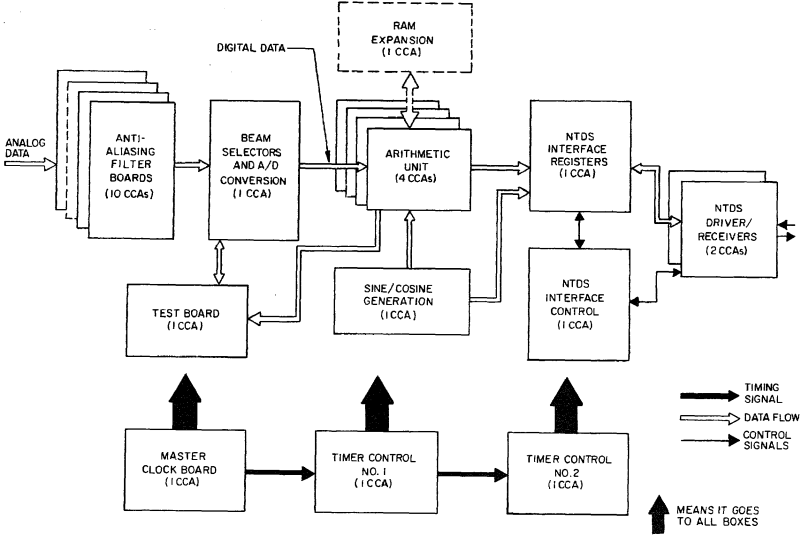
ANALOG MULTIPLEXERS.—Analog multiplexers can select from 82 separate input channels. The first 80 (numbers 0 to 79) input channels can accommodate beam inputs only. The remainder are used for test purposes. Beam 80 is used for external test input purposes and consists of a unity gain buffer and an antialiasing filter. Channel 96 is used for internal testing of the A to D process.

A TO D CONVERTER.—The A to D converter provides a 12-bit digital output at the rate of 32 kHz (64 kHz for expanded memory).

REGISTERS.—An 8-bit register is used to temporarily store the beam number for addressing the multiplexers. Another 12-bit register accepts the output of the A to D converter for temporary storage.

Arithmetic Unit CCA

The arithmetic unit (ARU) CCA contains the circuits for digital processing of the incoming beam signals. The four CCAs of this unit are interconnected via the back plane wiring. Each


RAM
EXPANSION
(1 CCA)
DIGITAL DATA
ANALOG DATA
ANTI-ALIASING FILTER BOARDS (10 CCAs)
BEAM SELECTORS AND A/D CONVERSION (1 CCA)
ARITHMETIC UNIT (4 CCAs)
NTDS INTERFACE REGISTERS (1 CCA)
NTDS DRIVER/ RECEIVERS (2 CCAs)
TEST BOARD (1 CCA)
SINE/COSINE GENERATION (1 CCA)
NTDS INTERFACE CONTROL (1 CCA)
TIMING SIGNAL
DATA FLOW
CONTROL SIGNALS
MASTER CLOCK BOARD (1 CCA)
TIMER CONTROL NO. 1 (1 CCA)
TIMER CONTROL NO. 2 (1 CCA)
MEANS IT GOES TO ALL BOXES

182.205.4

Figure 3-41.—IPU 1-1 circuit card functions and interactions.

ard contains multiplexers, registers, a × 12-bit multiplier, two 4-bit adder/sub- ctors, parity generator, and checkers and 1K 4-bits of random access memory (RAM). ur boards form a complete ARU for the U 1-1. The ARU uses odd parity for all data ored in RAM. The parity bit is stored as a 17th ta bit in RAM on the sine/cosine generator ard.

AM Expansion CCA

The RAM expansion CCA provides the tion of doubling the memory size of the U 1-1. The expanded memory allows the ocessing capacity to be increased from 32 to inputs. The CCA consists of 17, 1K by 1-bit AMs organized as 16-bit words and a parity t.

ne/Cosine Generation CCA

Various signals used in the processing/ nversion of analog/digital data by the IPU iginate on the sine/cosine generator CCA. e sine/cosine generation CCA includes the llowing:

- Sine/cosine generation logic
- The filter coefficient table
- Saturation logic
- A 1K-bit RAM for parity bit storage.

st CCA

The test CCA performs eight unique func- ns. These include:

- Power fault detection
- ARU testing
- Parity testing
- A to D testing
- *Power-up and master clear flag generation
- *Pilot tone flag generation
- Transmission of the computer-generated synchronization signals
- Buffering of signals to the internal test connector J06.

*A flag may be thought as the set/reset condition of a bit or series of bits, which will indicate a particular status or condition of a circuit or device. For example, a particular bit or pattern of bits being set to "1" state by the ADC Error Test Logic (figure 3-42) would indicate the presence of an A/D error.

Figure 3-42 shows a block diagram of the test functions of the CCA.

Master Clock CCA

The master clock CCA (refer to figure 3-41) provides all the timing signals required for IPU 1-1 operation. The source of the timing pulses is a 6.5536 MHz clock. This clock feeds a series of division circuits to achieve the necessary clock frequencies, the slowest of which has a repetition rate of 2 minutes.

A maintenance panel is connected to the CCA and facilitates testing and troubleshooting of the master clock CCA.

Timer Control No. 1 CCA

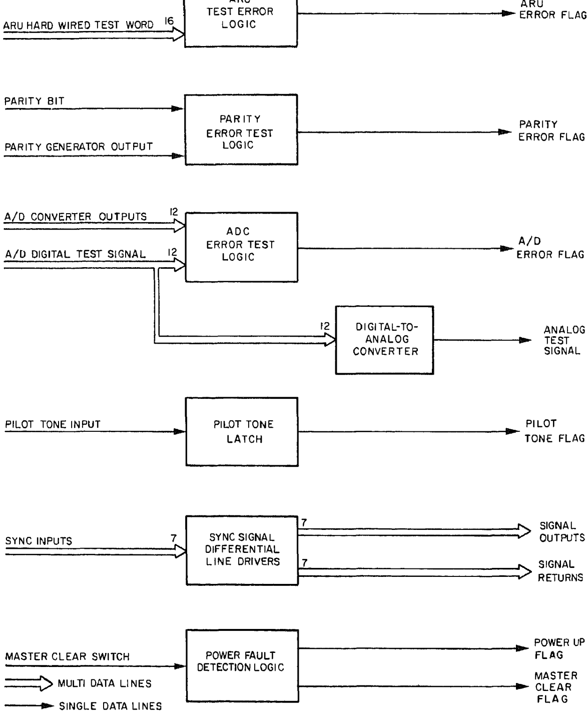
Timer control No. 1 CCA performs two main functions:

- The decoding of timing steps and states
- The generation of various control signals used for IPU operation.

Timer Control No. 2 CCA

Timer control No. 2 CCA performs the following functions:

- Control logic for loading all registers
- Logic for arithmetic test circuit
- Addressing for RAM and ROM memories.



182.205.5

Figure 3-42.—Test CCA block diagram.

e necessary logic that enables the IPU to mmunicate with a computer via an NTDS st interface. All data sent to or received from e host computer uses various "handshaking" gnals. ("Handshaking" was discussed in the O section of Part 1 of this module.)

TDS Interface Registers CCA

The NTDS interface register CCA contains e registers and multiplexers that control the o-way data flow through the NTDS interface.

TDS Driver and Receiver CCA

Two NTDS driver and receiver CCAs form e NTDS interface between the IPU and the st computer (AN/UYK-20). The function of e driver/receiver CCAs is basically the same as s discussed in the I/O section of Part 1 of this odule. Each NTDS interface driver/receiver ard consists of eight data line drives, and two ntrol line drivers, eight data line receivers, d two control line receivers.

POWER SUPPLY UNIT (PSU 26-1, 2, AND 3)

IIT DESCRIPTION

As indicated by its name, the primary rpose of the PSU is to provide dc voltages at

3-43) is a rack-mounted assembly and contains two Lamda Electronics Corporation power supply modules (figure 3-44). (When referring to the power supplies, you may encounter the short term "Lamda.") The assembly has a separate overvoltage protection module (figure 3-45). Two fans, configured with airflow sensors, ensure proper cooling of the PSU-26 unit.

The output voltages of power supplied to the equipment are as follows:

- PSU 26-1: +5 V dc at 27 amps and +/−15 V at 4 amps for one IPU 1-1
- PSU 26-2: +5 V dc at 35 amps and +/−15 V dc at 4 amps for two IPU 1-1 units
- PSU 26-3: +5 V at 35 amps and +/−15 V at 6.2 amps for one MIU

Input power is derived from an external 115 V 60 Hz single-phase source.

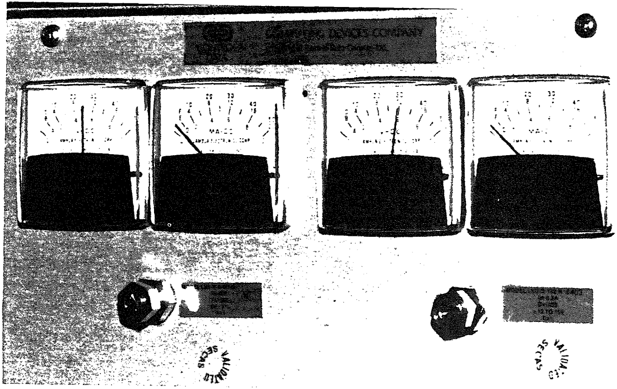
OPERATION

Once placed in service, the PSU 26 requires no operator intervention outside of normal maintenance procedures required by the Preventive Maintenance System (PMS). Table 3-7

Table 3-7.—PSU-26 indicators, switches, and connectors

J MARKING	REFERENCE DESIGNATION	FUNCTION
−15 V ADJ		A screwdriver adjustment lock-type variable potentiometer used to adjust the +/−15 volt dc output.
V ADJ		A screwdriver adjustment lock-type variable potentiometer used to adjust the +5 volt dc output.
/OFF	S1	A single pole, 2-position toggle switch used to connect primary power to the unit power supplies, fans and Elapsed Time Meter.
VER	DS1	A white lens indicator lamp which lights when ON/OFF switch S1 is set to ON.
	F1	A 7-ampere fuse, which provides primary power overload protection.
	—	A 3-pin connector used to connect primary power to the unit.
J2	J1 to J2	19 pin connectors supplying +5 and +/−15 volt levels.
	J3	2-pin connector, which appears as a short in normal condition, and as an open circuit if the air flow switches are in an alarm state.
PSED TIME	M1	An elapsed time meter which measures hours and tenths of hours when power is on.

182.206.3



182.206

Figure 3-43.—Power supply unit—front view.

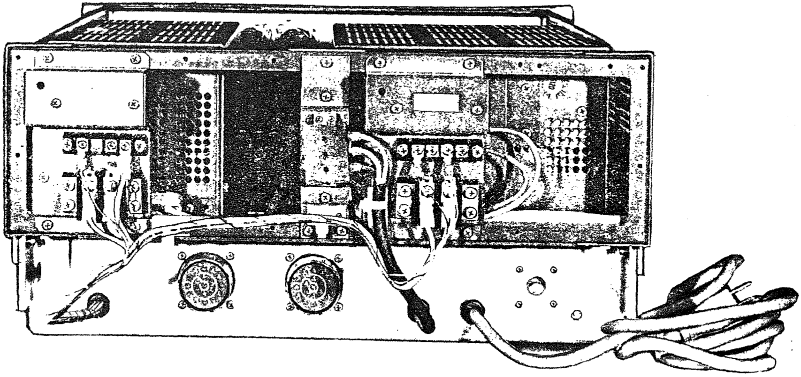
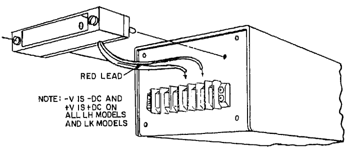
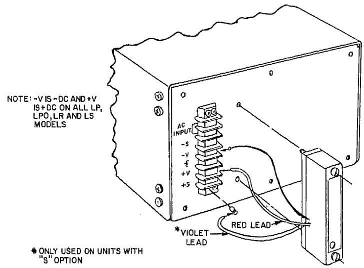


Figure 3-44.—Power supply unit—rear view.

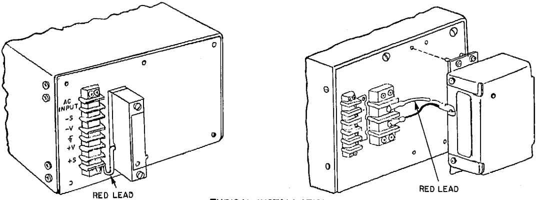
182.206.1


RED LEAD
NOTE: -V IS -DC AND +V IS +DC ON ALL LH MODELS AND LK MODELS

TYPICAL HORIZONTAL MOUNTING


NOTE: -V IS -DC AND +V IS+DC ON ALL LP, LPO, LR AND LS MODELS
AC INPUT
-S
-V
+V
+S
RED LEAD
*VIOLET LEAD
* ONLY USED ON UNITS WITH "S" OPTION

TYPICAL VERTICAL MOUNTING



TYPICAL INSTALLATION

182.206.2

Figure 3-45.—Overvoltage protector LMOV-7, 8, 9; typical installation.

intended to familiarize you with the physical lay-out of these items.

MAINTENANCE

The Lamda power supply modules are virtually trouble free. However, in the case of a failure, these modules must be repaired by the Lamda Corporation. A few minor adjustments can be made by the technicians, but these adjustments are generally limited to power supply level adjustments.

MODEL 40 TELETYPEWRITER EQUIPMENT

The Model 40 data terminals provide advanced facilities for entering, storing, displaying, editing, printing, sending, and receiving data in computer and communications systems. Significant features of the Model 40 terminals are: high speed, easy data preparation and editing, styles. These three styles and a brief description follow.

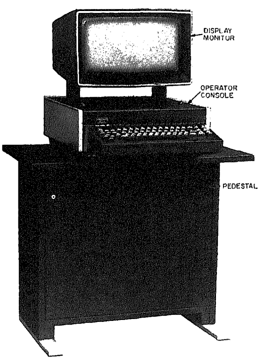
MODEL 40 KEYBOARD DISPLAY (KD)

The Model 40 KD shown in figure 3-46 displays messages on a monitor similar to a television set. A message typed locally on the keyboard is displayed on an antiglare screen, which makes the display easy to read. You can correct locally by using the editing controls (discussed later) prior to transmission. Received messages can also be displayed on the screen.

MODEL 40 KEYBOARD DISPLAY PRINTER (KDP)

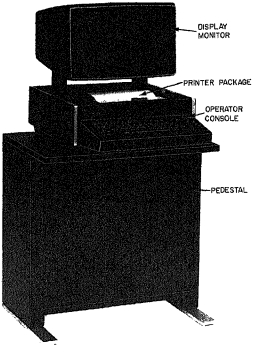
The Model 40 KDP is similar to a KD with the addition of a page printer. The KDP consists of the keyboard, display unit, and page printer.

The KDP pedestal configuration is shown in figure 3-47, with the printer located under the



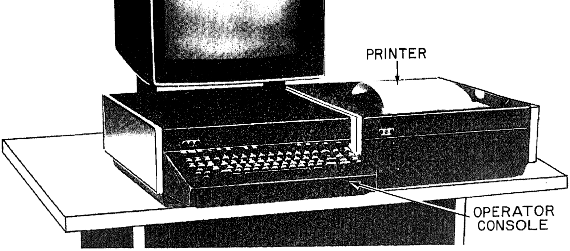
31.152

Figure 3-46.—Keyboard display (KD).



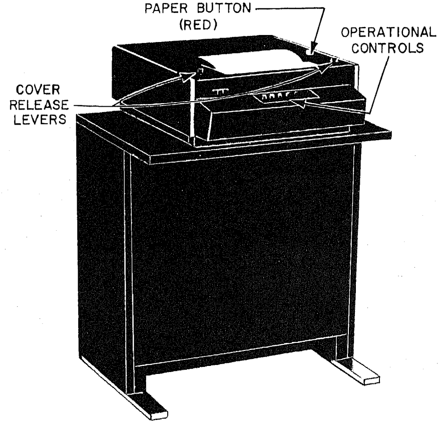
31.153

Figure 3-47.—Keyboard display printer (KDP)—pedestal mounted.



31.154

Figure 3-48.—Keyboard display printer (KDP)—table mounted.



31.155

Figure 3-49.—Receive only (RO).

the KDP is also configured as a table top model with the printer adjacent to the keyboard and display monitor. The printer of the KDP table top model may be located up to 50 feet from the unit.

The Model 40 KD and KDP contain a storage unit that "remembers" all characters and control functions indicated on the screen. Any errors shown on the screen can be corrected locally, which makes it possible to transmit error-free messages.

MODEL 40 RECEIVE ONLY (RO)

The Model 40 RO (figure 3-49) receives messages on a hard-copy page printer. The RO has its own set of operational controls.

LOCAL OPERATION (KD AND KDP)

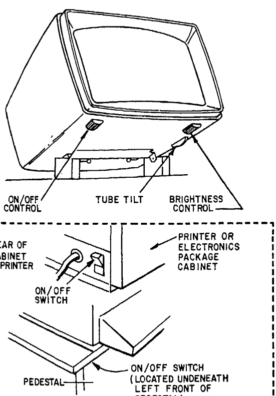
As shown in figure 3-50, power to the Model 40 KD and KDP is applied by switches located on the printer or electronic package cabinet, the pedestal and the display monitor. Power to the when the set is in receive or if PRINT ON LINE is selected to receive page copy. The keyboard is inoperative when the power to the display monitor is turned off.

The brightness control increases and decreases the intensity of displayed characters. Each character is formed on a 7 × 9 dot matrix (figure 3-51) and displayed on a flicker-free antiglare screen.

The unique tube tilt control allows the operator to adjust the display viewing angle for maximum clarity.

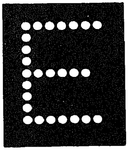
Cursor

The cursor is a light rectangular area on the screen that indicates where the next character will be displayed or the next function will take place. The cursor is always on the screen when the monitor is on. (After the display monitor power is turned on, a slight delay will be encountered after which the cursor and the No. 1 segment marker should appear as shown in figure 3-52.)


ON/OFF CONTROL
TUBE TILT
BRIGHTNESS CONTROL
REAR OF CABINET OR PRINTER
ON/OFF SWITCH
PRINTER OR ELECTRONICS PACKAGE CABINET
PEDESTAL
ON/OFF SWITCH (LOCATED UNDENEATH LEFT FRONT OF PEDESTAL)

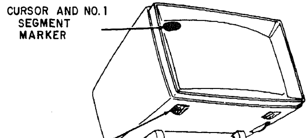
31.156

Figure 3-50.—Model 40 power and control switch.



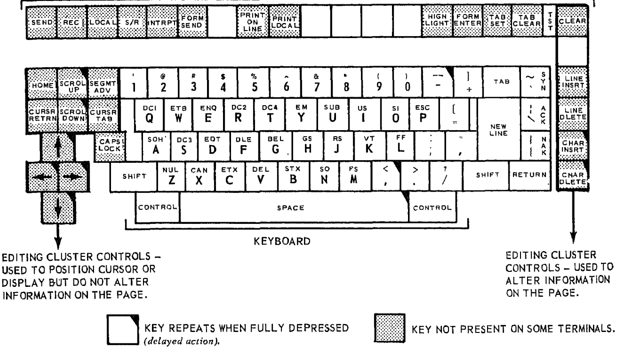
31.157

Figure 3-51.—Character formed on a 7 × 9 dot matrix.



31.158

Figure 3-52.—Cursor on display monitor.


SEND
REC
LOCAL
S/R
INTRPT
FORM SEND
PRINT ON LINE
PRINT LOCAL
HIGH LIGHT
FORM ENTER
TAB SET
TAB CLEAR
TST
CLEAR
HOME
SCROL UP
SEGMT ADV
CURSR RETRN
SCROL DOWN
CURSR TAB
CAPS LOCK
TAB
NEW LINE
SHIFT
RETURN
CONTROL
SPACE
LINE INSRT
LINE DLETE
CHAR INSRT
CHAR DLETE
KEYBOARD
EDITING CLUSTER CONTROLS – USED TO POSITION CURSOR OR DISPLAY BUT DO NOT ALTER INFORMATION ON THE PAGE.
EDITING CLUSTER CONTROLS – USED TO ALTER INFORMATION ON THE PAGE.
KEY REPEATS WHEN FULLY DEPRESSED (delayed action).
KEY NOT PRESENT ON SOME TERMINALS.

31.159

Figure 3-53.—Model 40 operator console.

When main power to the set and logic printer power is first turned on, the cursor may not be in the home position, or random characters may be displayed on the screen. This is caused by power variations when power to the entire set is turned on. To clear the display screen and home the cursor, press the HOME and then CLEAR keys. The HOME and CLEAR keys are discussed in the following paragraphs.

OPERATOR CONSOLE

In addition to the standard ASCII keyboard arrangement, the Model 40 has several unique control keys. Figure 3-53 shows the Model 40 operator console. The data entry keys, data editing keys, and data communication keys are clearly separate from one another for ease and efficiency of operator use. The discussion that follows explains and illustrates the various features of the operational mode controls, editing controls, and the keyboard.

Operational Mode Controls

The operational mode controls (top row of keys shown in figure 3-53) light when pressed to indicate the operational mode of the terminal. The keyboard and editing controls will not operate in the SEND or RECEIVE mode. Each of the function control keys is defined as follows:

- SEND—Pressing this key places the keyboard directly on-line. Pressing any key in the typewriter field causes that character to be sent on-line. If a cursor control key, insert, or delete key is pressed, no character will be sent. If no key is pressed within 15 seconds of going into the SEND mode, the set will switch back to the RECEIVE mode.

- REC—This key lights when power is turned on. In the RECEIVE mode the printer copies the receive line, and the keyboard is inoperative.

ommunication to take place.

- INTRPT—Stops transmission from re- ote device by sending interrupt signal.

- FORM SEND—Overrides the send options ssociated with the SEND key. Causes all data o be sent as displayed, whether protected or ighlighted, including tab stops, when the END key is pressed.

- PRINT ON-LINE—Puts terminal in re- ceive mode, unless the SEND key is pressed. ermits terminal to receive data on the printer nd the display module, unless the display module turned off. Data is displayed from the cursor ocation to the end of display memory if display on. If SEND key is pressed, PRINT ON-LINE auses sent data to be printed as sent, according o the send option.

- PRINT LOCAL—Causes printer to print ll data in display memory, regardless of send ption, from the cursor location to the end of isplay memory.

- HIGHLIGHT—Causes characters that ollow to be displayed as highlighted char- cters.

- FORM ENTER—Puts terminal in pro- ected data mode, during which all data entered vill be displayed as protected data. Operation of he CLEAR key clears protected and unprotected ata from memory. Operation of the editing keys ffects both protected and unprotected data.

- TAB SET—Sets tab stops at the cursor ocation on that line and all lines below to end f display memory.

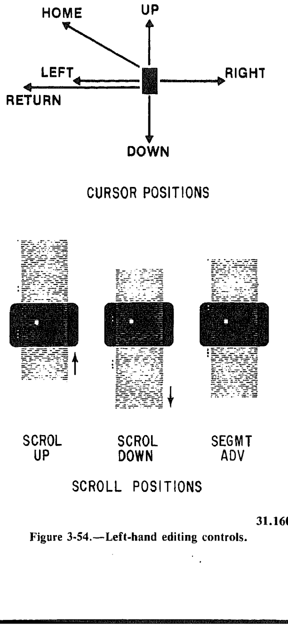
- TAB CLEAR—Clears all tab stops from he cursor location to the end of the line, on that ine and all lines below to the end of display nemory.

- TST—Initializes internal testing functions or the unit.

ENTER and then the CLEAR keys.

Left-Hand Editing Controls

These keys are used to position the cursor or displayed data; they do not alter information on the page. Additionally, the left-hand editing controls operate only in the local mode. Figure 3-54 shows the various positions of the cursor and scroll when one of the left-hand editing controls is pressed. The left-hand editing controls



31.160

Figure 3-54.—Left-hand editing controls.

- HOME—Causes the first segment to be displayed and moves the cursor to start of first line.

- CURSR RETRN—Moves the cursor to start of line.

- Up arrow, left arrow, right arrow and down arrow (repeatable)—Moves the cursor up, left, right and down, respectively.

- SCROL UP AND SCROL DOWN (repeatable)—Moves displayed data up and down, respectively.

- SEGMT ADV—Removes the 24 lines being displayed and displays the next whole 24 line segment of 25 lines each. The three segments contain a total of 72 lines; each line can contain a maximum of 80 characters.

- CURSR TAB—Moves the cursor to the first tab stop on the right, to the start of the

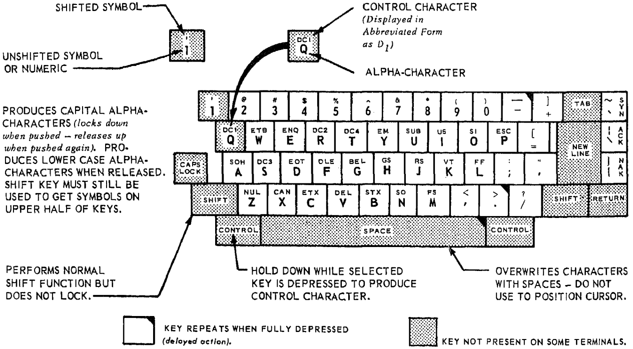
Right-Hand Editing Controls

The operation of the right-hand editing controls can be affected when protected data or tab marks are present. These keys alter information on the page and operate only in the local mode. The right-hand editing controls are defined as follows:

- LINE INSRT—Moves unprotected data down one line, which creates a line of space on the line the cursor is on. This does not occur if there are no lines of space at the end of the display memory or if there are no lines of space above the first line below having protected data in it.

- LINE DLETE—Clears unprotected data from the line the cursor is on and moves all unprotected data displayed below up one line.

- CHAR INSRT (repeatable)—Moves unprotected data one character to the right so that


SHIFTED SYMBOL
UNSHIFTED SYMBOL OR NUMERIC
CONTROL CHARACTER (Displayed in Abbreviated Form as D_1)
ALPHA-CHARACTER
DC1 Q
PRODUCES CAPITAL ALPHA-CHARACTERS (locks down when pushed – releases up when pushed again). PRODUCES LOWER CASE ALPHA-CHARACTERS WHEN RELEASED. SHIFT KEY MUST STILL BE USED TO GET SYMBOLS ON UPPER HALF OF KEYS.
! 1 @ 2 # 3 $ 4 % 5 ^ 6 & 7 * 8 (9) 0 — -] + TAB ~ ` SYN
DC1 Q ETB W ENQ E DC2 R DC4 T EM Y SUB U US I SI O ESC P [= NEW LINE | \ ACK
CAPS LOCK SOH A DC3 S EOT D DLE F BEL G GS H RS J VT K FF L : ; " ' } { NAK
SHIFT NUL Z CAN X ETX C DEL V STX B SO N FS M < , > . ? / SHIFT RETURN
CONTROL SPACE CONTROL
PERFORMS NORMAL SHIFT FUNCTION BUT DOES NOT LOCK.
HOLD DOWN WHILE SELECTED KEY IS DEPRESSED TO PRODUCE CONTROL CHARACTER.
OVERWRITES CHARACTERS WITH SPACES – DO NOT USE TO POSITION CURSOR.
KEY REPEATS WHEN FULLY DEPRESSED (delayed action).
KEY NOT PRESENT ON SOME TERMINALS.

31.161

Figure 3-55.—Keyboard.

- CHAR DLETE (repeatable)—Clears unprotected character at the cursor location and moves all unprotected data displayed on the right one character position to the left.

Keyboard

Figure 3-55 shows the remainder of the operator console, which resembles a standard keyboard arrangement. Pressing a key by itself generates either the character marked on the lower half of the key or the control marked in the center of the key. Pressing a key with the SHIFT key generates either the uppercase equivalent of the character marked on the lower half or the character marked on the top half of the key. Pressing a key with the CONTROL key generates the control marked on the key.

PRINTER OPERATION

The page printer (figure 3-56), if present, provides a hard copy of messages originated locally or messages transmitted or received on-line. The PRINT LOCAL and PRINT ON LINE keys control the operation of the page printer. These keys are located just above the keyboard.

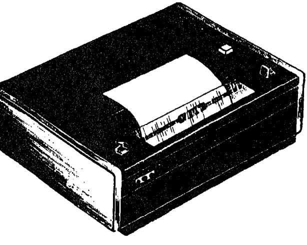
message ending character.

The PRINT ON-LINE key, when pressed (lights), provides a printed copy of any data transmitted or received on-line. This key will light until pressed again.

The PAPER button, which is red, is located on top of the printer. When pressed, the paper in the page printer advances until the button is released. The PAPER button lights when an out-of-paper condition exists and extinguishes when the paper supply is replenished.

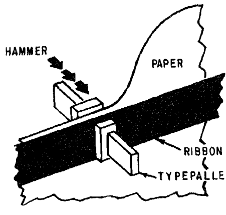
The Model 40 printer module prints characters by means of individual typepallets (figure 3-57) in an endless revolving carrier belt. This method provides high-speed operation without losing the character clarity and changeability advantages of an impact type of box printer.

The printing is produced by 80 print hammers; one hammer for each print position. They strike the paper into the ribbon and onto the typepallets as the typepallets "fly" by on their continually moving carrier. This process produces crisp impact printing of full characters—not dots arranged to look like characters. With 80 print hammers, each hammer is performing only 1/80th of the work, at 1/80th of the printing speed. This means longer printer life and less maintenance, even though the printing speed is much higher than that of conventional printers.



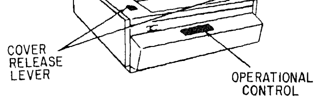
31.162

Figure 3-56.—Page printer.



31.163

Figure 3-57.—Individual typepallet and hammer.



31.164

Figure 3-58.—Receiver-only page printer.

Rapid Print-Out Rate

The full ASCII printer can print up to 3.7 lines per second with up to 80 characters per line, for a maximum capability of almost 300 characters per second.

RECEIVE-ONLY (RO) PAGE PRINTER OPERATION

The RO page printer, (figure 3-58) provides a hard copy of messages received on-line. The RO set has its own set of operational controls and are defined as follows:

- INTRPT—Sends a reverse channel signal to halt the remote sender if reception becomes garbled or unwanted.

- TRANS START—Sends a discrete calling code to a remote device when the terminal is on-line. Generates test data when the terminal is off-line.

- IN SERVICE—Terminal ready, that is, power on, no/low paper supply, and so forth.

- DATA ERROR—Illuminates on receipt of character with parity error.

The RO printer terminal also has a test data generator. With this feature the operator can press a button and generate a sequence of characters that will test the terminal for proper operation.

The printer normally prints six lines per inch, but the operator can select three lines per inch by

Built-In Diagnostics

As reliable as the Model 40 is, casualties sometimes occur. To facilitate maintenance, the display module has built-in diagnostics to isolate malfunctions.

Should a malfunction occur in the display module, a series of neon glow tubes will be visible from the outside of the unit. These indicators are actually mounted on circuit cards inside the unit. A quick glance at these neon tubes will indicate which card is not functioning properly.

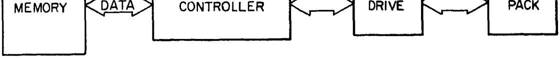
You can also check the terminal logic by pressing pushbuttons on the circuit cards inside the terminal controller and observing test patterns on the display screen. The card that does not display its proper pattern has the defective component.

You can also check the operator console for proper operation. Combinations of keys, pressed below their normal downstop, will light indicators on the console if the console is working properly.

Once the trouble is isolated, you can easily exchange either the circuit cards or the whole module to accomplish the required maintenance. This is because the display module, printer, operator console, and the circuit cards feature a combined mechanical-electrical connection for rapid replacement.

DISK STORAGE SYSTEM

In Part 1 of this module, you were introduced to the purpose of a typical disk storage device. Disk systems fill the gap between fast but somewhat costly computer memory (cores, ICs, thin film, and so forth) and inexpensive but slower magnetic tape. Disks are called random-access devices, because any piece of data stored on the disk can be retrieved in virtually the same amount of time, no matter where it is located. Data can be randomly accessed rather than having to sift through masses of unwanted data.



182.207

Figure 3-59.—Disk system components.

DESCRIPTION OF DISK SYSTEMS

When you hear the term "disk" used, as in "the data will be stored on disk," a disk system s actually being referred to. A disk system is comprised of several different components, each of which performs specific functions. The components comprising a typical disk system are:

- The disk pack
- Disk drive
- Disk controller.

Functionally, these components are arranged as ndicated in figure 3-59. Although the components shown are separated by their function, disk drives and disk packs are always in the same physical enclosure. Also, the controller may be ocated in the disk park/drive enclosure as well. However, the controller will be a separate unit in the majority of subsystems you will encounter.

Generally, the following sequence of events occur when data is stored on the magnetic surface of the disk:

- The controller accepts data from the host computer, transforms it in some manner (called formatting), and transmits it to the disk drive.
- The disk drive locates the position on the actual storage medium (disk pack) where the data is to be stored and records it there. The process shown in figure 3-59 is reversed when data is read from a disk system.

PHYSICAL DESCRIPTION OF DISK SYSTEM COMPONENTS

A disk pack (which is composed of a number of disk platters) was described in Part 1 of this module. If you are not familiar with this information, you should review the appropriate pages of Part 1.

The disk drive contains the necessary machinery to spin the disk pack at a high rate of speed (usually about 3600 rpm). The disk drive also contains an array of read/write heads and electronic and electromechanical devices necessary to support the reading and writing of data.

DISK DRIVE FUNCTIONS AND CONCEPTS

As we just stated, the basic functions of a disk drive are to spin the disk pack at a high rate of speed and to effect the movement of the read/write head assemblies to read/write the required data on the disk surface. Some of the concepts and terms applicable to disk storage systems are discussed in the next paragraphs.

Seeking

Seeking is the process of moving the read/write head assemblies to the desired data track.

Seek Time

Seek time is the time that a seek operation takes. This time can vary from zero (if the heads are already at the desired track) to the time it takes to get from the outermost track to the innermost (or vice-versa).

Fixed/Moving Head

There are two types of read/write head arrangements: fixed head and moving head. In

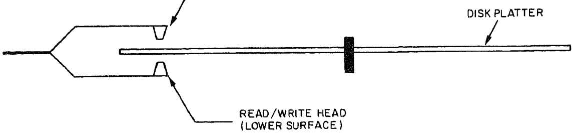


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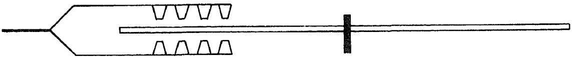
Figure 3-60.—Moving head arrangements.



182.207.2

Figure 3-61.—Fixed head arrangements.

the moving head arrangement (figure 3-60), which is the type you will be working with, the read/write heads (one per disk pack surface) are mounted on a moveable arm that positions the head assembly to various places across the disk surface. Figure 3-60 shows the relative positions of the heads in relation to the disk pack surface (one platter shown). As you can see, the heads are mounted on a common arm and move across the disk surface together. This movement is not a continuous smooth movement but, rather, takes place in incremental steps. Only one head is active at any one instant even though the disk pack may have many surfaces and read/write heads. The process of selecting which head will be active is done electronically and is called head-switching and/or head-selection.

In the less common arrangement, called fixed head arrangement (figure 3-61), there are a number of heads per disk surface mounted on a stationary arm. Rather than moving the arm assembly, a particular head is activated electronically to accomplish the read/write operation.

FORMAT OF DATA ON DISK

In Part 1 of this module, we discussed a typical disk storage device to familiarize you with the concepts involving the storage of large amounts of data. The terms involved with the formatting of data on the disk recording surfaces are restated in the following paragraphs. It is very important that you understand these terms because you will need to know their meanings when you study the materials presented later in this section.

Data Track

The first concept is that of a data track on a disk surface. To visualize what a track is, first remember that the disk platter is always spinning very fast. If it is not, the computer cannot communicate with the disk. A track is the area of the disk surface that passes under a read/write head while the head is in one of its positions. There are as many tracks on the surface of the disk as there are possible positions of the read/write head.

that can be read or written without moving the read/write head assemblies. In a disk pack that contains more than one platter, a cylinder consists of a given track on the uppermost data surface (not all platters are used to record data) and all corresponding data tracks on the platters below it. The number of cylinders is equal to the number of tracks on a single data surface.

Sector (Record)

A sector is only a segment of a track. Its size is determined by hardware. A sector corresponds to the smallest amount of data that can be written onto a disk during any one access. For instance, you would not go to the trouble of locating a given track on the disk and selecting the correct read/write head just to write one bit of data. (It is theoretically possible, but very inefficient.) All sectors contain the same number of bits, and there are an equal number of sectors per track. The number of sectors per track depends on the manufacturer of the disk drive unit and how the unit is used.

Latency

Latency is the time it takes to access a given sector (remember, sector is just a segment of a track) once the heads have arrived at the desired track. Latency varies inversely with the speed of rotation of the disk and ranges from zero (assuming the sector happens to be immediately under the read/write head when it gets to the track) to one full rotation of the disk pack (277.7 μsec 3600 rpm assumed). The average latency is, therefore, the time it takes for one half of a rotation of the disk pack (138.85 μsec).

Transfer Rate

Transfer rate is the number of bits per second (or equivalent units) that can be sent or received by the disk drive.

Access Time

Access time is the elapsed time from when a piece of data is requested by the computer until the computer receives it. Access time depends on

DISK CONTROLLER FUNCTIONS

The disk controller performs a variety of functions that facilitate the reading and/or writing of data. These functions are as follows:

Overlap Seek

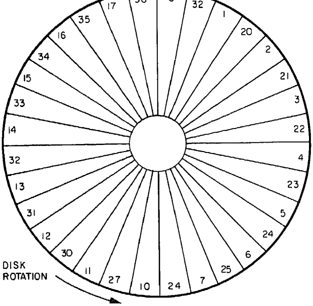
Depending on how a controller is configured, it is possible for one controller to "oversee" more than one disk drive. In cases where more than one disk drive is under the influence of a controller, a function called an overlap seek may be performed. This simply means that while one disk drive is reading or writing data, the controller can order another disk drive to seek a data track. This action greatly speeds up the ability of a computer to process data, since the computer does not have to wait for one function (the reading or writing of data) to terminate before performing another (seeking a track).

Serial/Parallel Conversion

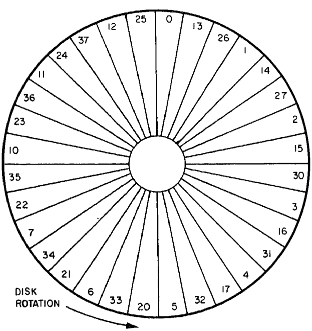
A necessary function of the controller is the serial-parallel (or vice versa) conversion of data. As an example, in many disk systems the computer will send a multiple-bit word to the controller. In the case of a 16-bit word, the computer will send all 16 bits to the controller at the same time over 16 different lines (parallel data transfer). To record this word on the disk pack, the drive must receive one bit at a time. The controller will temporarily store the received parallel word and send it to the drive in a serial data stream. The above process is reversed when data is to be read from the disk.

Error Checking

The controller can perform error checking of the data. For each sector of data written, the controller will cause an extra word to be written on the disk pack. (This word is called a Cyclic Redundancy Check (CRC).) The CRC is a mathematical function of the bit pattern of its associated sector. When data is read back from the disk pack, the controller recomputes the CRC word, compares it with the one previously



DISK SECTOR INTERLEAVING 2:1



DISK SECTOR INTERLEAVING 3:1

NOTE: SECTOR NUMBERS IN OCTAL

182.207.3

Figure 3-62.—Disk sector interleaving.

ecorded and generates an error signal if the two CRCs differ. A mismatch between the CRC vords would indicate that one or more of the lata bits was changed.

Buffering

Buffering enables a small amount of data hat is read to be stored in the controller until he computer is ready to accept it. The buffering apability of different types of controllers will ary. Buffering allows the computer to finish an peration while the buffer is filling. This prevents he computer from having to drop everything nd divert its attention to the disk only.

Disk Sector Interleaving

Disk sector interleaving is a technique used o slow the average transfer rate of the disk rive. This technique is used when the disk drive nit has the capability of transferring data at a faster rate than the host computer is able to accept it. When this technique is used, data is recorded and/or read from every other sector (2:1 interleaving), every third sector (3:1 interleaving), and so on. Figure 3-62 illustrates the interleaving arrangements for 2:1 and 3:1 interleaving. Various configurations of formatters and disk drives may use different interleaving intervals (such as 4:1).

DIGITAL SYSTEMS CORPORATION (DSC) DISK CONTROLLER, MODEL 3985

The DSC Model 3985 disk controller (figure 3-63) is a multiprocessor-based device. It provides for the transfer of data between a maximum of two host computers and up to eight disk drive units. This is the maximum configuration for the Model 3985 controller and is dependent upon the quantity of host interface and disk interface circuit cards installed. The design of the controller allows each host computer to independently (two host computer configurations) read and write data to and from the disk drive unit with maximum efficiency and accuracy of data transfer.

The basic makeup of the controller is shown in figure 3-64. Its present maximum configuration consists of:

- Two host computer interface cards, which allow simultaneous operation with two host computers.
- Four disk drive interface circuit cards, which allow the transfer of data and the control of up to eight disk drive units.
- One front panel interface card, which provides for a diagnostic capability, front panel operations, and system monitoring during normal operation.
- A power supply assembly, which provides the necessary voltages for controller operation.
- A front panel assembly, which allows for control and monitoring functions.
- A fan assembly (not shown), which provides for unit cooling.

The host interface, disk interface, and front panel interface may have varying part numbers assigned to them. These varying part numbers make the circuit cards compatible, partially compatible, or noncompatible. If you encounter problems in interchanging disk drive units, contact the technical manuals for your particular site installation to determine card compatibility status.

CAPABILITIES

In addition to the functions we pointed out in the previous discussion, the DSC Model 3985 disk controller is capable of the following:

- Providing assistance via messages on the LED display on the front panel when the "HELP" pushbutton is activated.
- The ability to format enable and override write protect areas on individual disk drives.
- Performing commands and data transfer, command validation, electronic error correction, and operator-initiated control, monitoring, and diagnostics of system operation.

6-1-1	Assy: Front Panel	* 40-0056-01
-2	Lamp: Green (3)	39-3332-00
-3	Lamp: Neon	39-1537-00
-4	Spacer: Nylon (2)	15-2206-40
-5	Screw: Flat Head, Phillips (4)	MS 24693S-24
-6	Hinge Block: Upper	40-5013-01
-7	Hinge Block: Lower	40-5013-02
-8	Lamp: Red	39-3331-00

* Indicates repair part

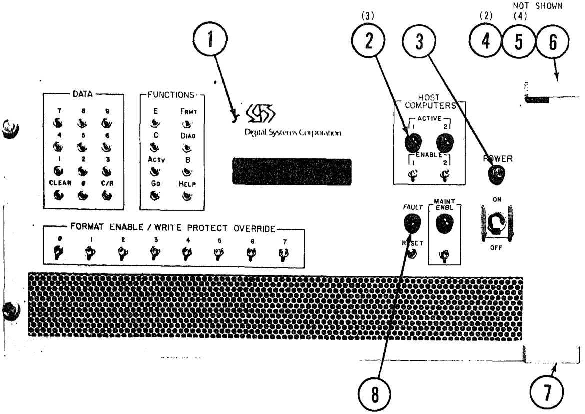


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Figure 3-63.—Digital Systems Corporation Disk Controller, Model 3985.

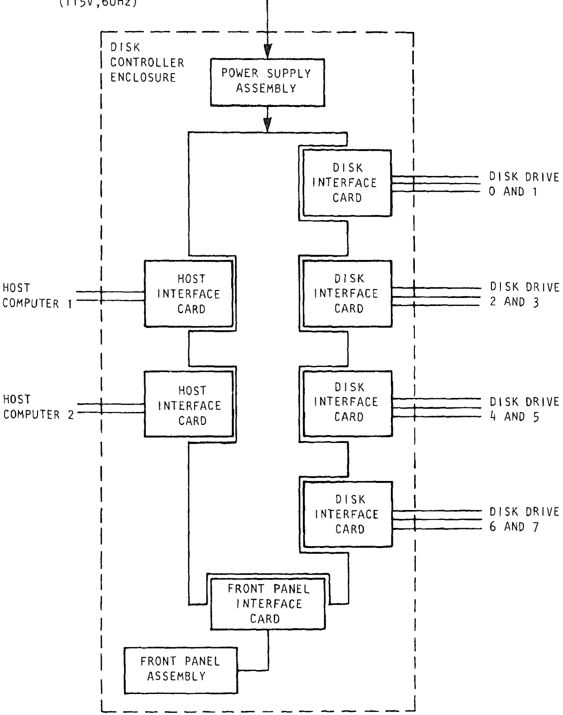

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Figure 3-64.—Controller functional design diagram.

- In the event of an error associated with a particular drive unit, the controller automatically reserves a drive to allow error recovery.

- Assigning alternate cylinder numbers, which allow from one to four defective cylinders on a disk pack to be skipped without performance degradation.

- Formatting an entire disk pack or any number of sectors requested via the host computer or the controller front panel with 1:1, 2:1, 3:1 or 4:1 interleaving and active head staggering with 2:1 and 4:1 interleaving automatically.

- Performing seek and automatic seek operations concurrent with other operations.

- Supporting data strobe early/late and servo plus/minus to recover marginal data.

- Supporting "return to 0" and "fault clear" for error recovery.

- Prereading or writing 0s in the unused portion of sectors when ignoring sector boundaries.

- Providing an internal program load command used for "bootstraping" the computer.

CONTROLS AND INDICATORS

The controls and indicators used for operating the DSC Model 3985 disk controller are located on the front panel of the unit. Refer to the applicable technical manual for a description of their use.

OPERATING THEORY

As we discussed earlier, the DSC Model 3985 disk controller can transfer data between a maximum of two host computers and up to eight disk drive units. The controller receives instructions from the host computer and responds to these instructions. This results in the ability to store and/or recall large quantities of data to/from the disk drive units.

next paragraphs.

Controller Interface Description

The interface description of the Model 3985 disk controller can be divided into two general areas:

- Controller external interface description
- Controller internal interface description.

An introductory explanation of these two areas follows.

External Interface Description

The input/output and power connections of the controller are made via 17 connectors located on the rear panel of the unit (figure 3-65). Four of the connectors provide an interface with the host computer, twelve interface with the disk drives, and one is used for ac power input.

CONTROLLER TO HOST COMPUTER INTERFACE.—Data read from the disk drive unit is transferred to the host computer as an input data (ID) function (handshaking). Status information is transferred as external functions (EF) by appropriate control signals between the controller and host computer.

Data transmitted from the host computer to the controller is sent as an output data (OD) function. Command information is transmitted as external functions (EF) via appropriate control signals between the controller and host computer.

Any data transfer, whether it is from the host computer to the controller or vice-versa, involves the use of appropriate handshaking signals.

Controller to Disk Drive Interface

Signals between the controller and the disk drive(s) are carried bidirectionally on I/O cables called A and B cables. Four A cable connectors and eight B cable connectors are contained on the rear panel of the controller. Each A cable

FIGURE/INDEX	NOMENCLATURE/DESCRIPTION	PART NUMBER
6-2-1	Screw: Slotted, Pan Head (4)	MS 35223-63
-2	Cable Clamp: Chassis Rear Panel	40-5015-01
-3	Handle: Chassis Rear Panel (2)	17-1624-00
-4	Screw: Flat Head, Phillips (4)	MS 24693S-48
-5	Screw: Pan Head, Phillips (8)	MS 35206-14
-6	Finger Guard: Fan (2)	50-5099-00
-7	Fuse Holder	34-9220-00
-8	Fuse: 5A Slo Blo (Not Shown)	34-0500-02
-9	Plug: Chassis Mount 115 Vac	26-5115-00

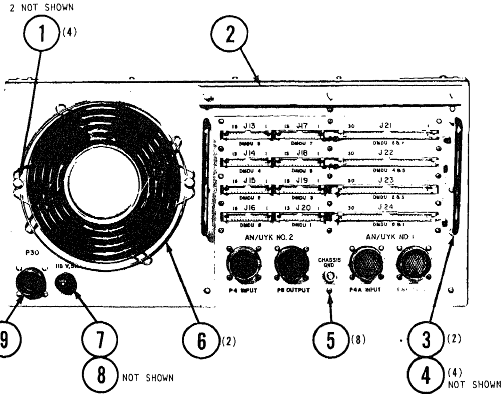

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Figure 3-65.—Controller chassis (rear view).

information to and receives status information from the disk drive unit via the A cable. The controller also sends unit clock and data to and receives status information and read data from the disk drive unit via the B cable.

Internal Interface Description

The internal interface for the host, disk, and front panel interface cards is provided by the high- and low-speed buses (figure 3-66). If two host interface cards are installed, two high-speed buses exist, one for each card. The low-speed bus provides the interface structure for the front panel.

HIGH-SPEED BUS.—The high-speed bus connects the host and disk interface cards. Each bus is dedicated to a host interface card (two maximum) and carries data to and from all four disk interface cards (figure 3-66). Since both host interface cards have a dedicated high-speed bus, transfer of data between different host and disk interface cards can be performed simultaneously. However, the disk interfaces are restricted to working with one high-speed bus at a time. Data transfers are made in 8-bit bytes. All information enabled on the high-speed bus is synchronously timed and transferred at the rate of about 800 nanoseconds per byte.

LOW-SPEED BUS.—The low-speed bus is bidirectional and is used for sending control, timing, command and status information between the cards connected to it. Transfers are made in 8-bit or 10-bit bytes at the rate of 200 nanoseconds per byte.

In the maximum configuration of a controller, the following conditions could exist:

- Either of the host interface cards could control the bus.
- The front panel interface can act as a slave to the bus.
- Any of the four disk interface cards can act as slaves to the bus.

host interface must bid for the bus before a transaction involving the bus can be completed. The front panel interface grants use of the bus to the first bidder as soon as the bus is available. To avoid simultaneous requests for the bus, the two host interfaces are clocked out of phase.

FUNCTIONAL DESCRIPTION

An overall functional block diagram of the Model 3985 disk controller is illustrated in figure 3-66. This figure shows the controller in its maximum configuration. An introductory analysis of the interrelationship of figure 3-66 follows and is divided into six areas:

- Host interface
- Disk interface
- Front panel interface
- Front panel assembly
- Power distribution
- Controller cooling (not shown).

Host Interface

The host interface is an independent operated computer. It facilitates data buffering, burst error processing, and data transfer between the associated host computer and the disk interface via the high-speed bus.

The host interface (foldout 3-2, at the end of this chapter) is divided into the following functional areas:

- Computer interface
- Data buffer
- Microprocessor
- High-speed bus interface
- Low-speed bus interface
- Burst error processor.

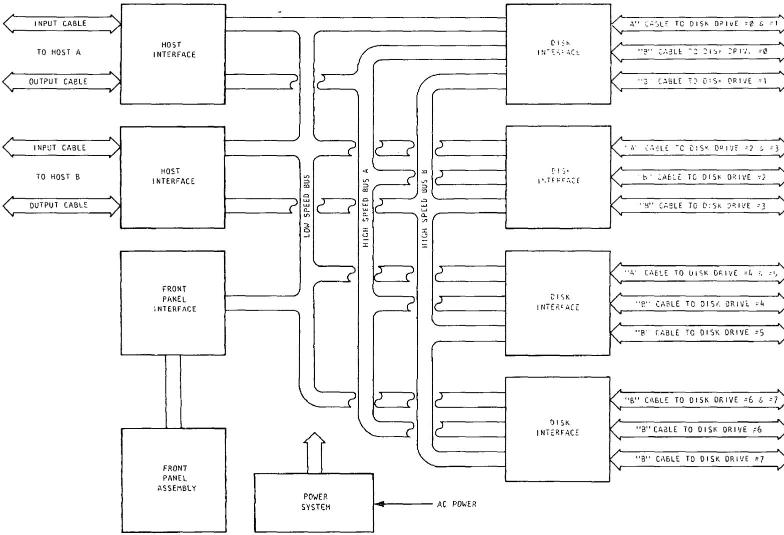
INPUT CABLE
TO HOST A
OUTPUT CABLE
HOST INTERFACE
INPUT CABLE
TO HOST B
OUTPUT CABLE
HOST INTERFACE
FRONT PANEL INTERFACE
FRONT PANEL ASSEMBLY
POWER SYSTEM
AC POWER
LOW SPEED BUS
HIGH SPEED BUS A
HIGH SPEED BUS B
DISK INTERFACE
"A" CABLE TO DISK DRIVE #0 & #1
"B" CABLE TO DISK DRIVE #0
"B" CABLE TO DISK DRIVE #1
DISK INTERFACE
"A" CABLE TO DISK DRIVE #2 & #3
"B" CABLE TO DISK DRIVE #2
"B" CABLE TO DISK DRIVE #3
DISK INTERFACE
"A" CABLE TO DISK DRIVE #4 & #5
"B" CABLE TO DISK DRIVE #4
"B" CABLE TO DISK DRIVE #5
DISK INTERFACE
"B" CABLE TO DISK DRIVE #6 & #7
"B" CABLE TO DISK DRIVE #6
"B" CABLE TO DISK DRIVE #7

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Figure 3-66.—Controller functional block diagram.

COMPUTER INTERFACE.—The computer interface, under control of the microprocessor and the host computer, facilitates data transfer between the host computer and the data bus. The computer interface consists of NTDS Fast compatible receivers and transmitters, input and output latches, and associated control logic.

DATA BUFFER.—The data buffer consists of a random access memory and a set of transceivers. The data buffer temporarily stores data that is transferred from the host computer to the high-speed bus during a write operation, or from the high-speed bus to the computer during a read operation. It also stores data that is transferred from the host computer during a verify operation.

The data buffer is also used for the storage of the interleaving control table and the alternate cylinder table. (The alternate cylinder table is used to store the number(s) of the defective cylinder(s) from a disk pack.)

MICROPROCESSOR.—The microprocessor provides for basic control of the host interface circuitry. It includes a microprogram sequencer, a programmable read only memory (PROM), which stores the microcode required for implementing the functions of the microprocessor, and an ALU. The microprocessor performs command control and interpretation functions and checks the received command for validity.

HIGH-SPEED BUS INTERFACE.—The high-speed bus, under control of the microprocessor and the appropriate disk interface, facilitates the transfer of data between the data and high-speed buses. It consists of two sets of latches. One set transfers data from the high-speed bus to the data bus, and the other set transfers data from the data bus to the high-speed bus.

LOW-SPEED BUS INTERFACE.—The low-speed bus interface provides for the transfer of control information from the host microprocessor to the low-speed bus. The low-speed bus interface also provides for the transfer of status information from the low-speed bus to the host microprocessor.

- Error detection during read, write, and verify operations.
- Error correction during read operations. The burst error processor can correct errors that have occurred on the data areas of any given sector on the disk pack.

For error detection(s) the burst error processor is under control of the disk microprocessor. For error correction(s) the burst error processor is under dual control of the host/disk microprocessors. When the disk microprocessor is not using the burst error processor, the control lines of the burst error processor are set for error correction. The control lines from the host microprocessor actually enable the burst error processor to perform error correction.

Disk Interface

The disk interface, much like the host interface, is an independent operated computer. The disk interface facilitates the transfer of data and control signals between the selected disk drive and the host interface.

The disk interface (figure 3-67) is divided into the following functional areas:

- High-speed bus interface
- Low-speed bus interface
- Disk data processor
- Disk drive control
- Data converter
- Sector locator
- Drive unit interface.

A brief description of these functional areas follows. You can obtain more detailed information from the Model 3985 technical manual.

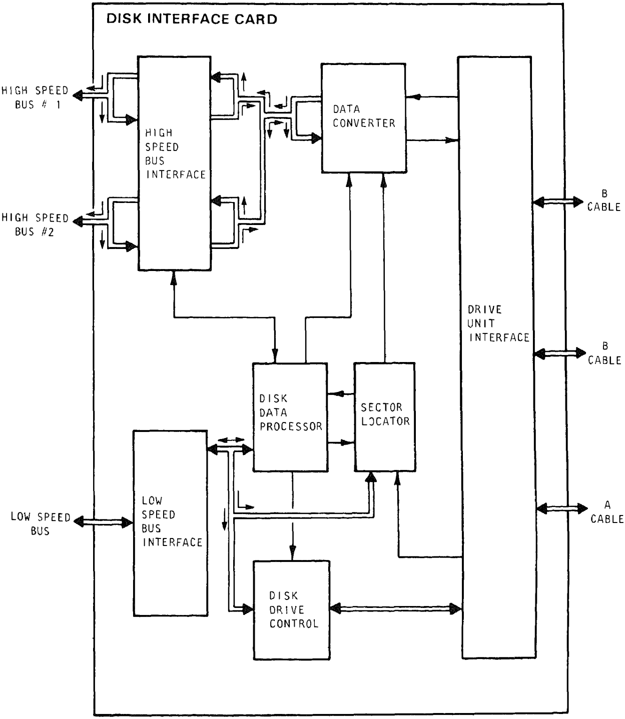

Figure 3-67.—Disk interface functional block diagram.

- Provides for the transfer of data to and from the appropriate host interface and the data converter.

- Provides for the data overrun and burst error processor signals from the appropriate host interface to the disk data processor.

- Provides for the transfer of control information from the disk data processor to the appropriate host interface.

LOW-SPEED BUS INTERFACE.—The low speed bus interface contains logic which facilitates the transfer of the following information:

- Control information from the low speed bus to the disk drive control.

- Status information to the low speed bus from the disk data processor.

- Control information from the low speed bus to the sector locator.

DATA CONVERTER.—The data converter accomplishes parallel-to-serial conversion of the data (8-bit) received from the high-speed bus interface. This data is then transferred to the drive unit interface. In the opposite direction, serial data from the drive unit interface is converted to parallel data (8-bit) for transfer to the high-speed bus interface. Selection of the conversion process is initiated by the sector locator and is performed by the disk data processor. The conversion process is synchronized with the disk drive unit by the read or write clock signal received via the drive unit interface.

DISK DATA PROCESSOR.—The disk data processor oversees the transfer of data between the controller and disk drives. To accomplish its task, the disk data processor incorporates transceivers, a microprogram sequencer, and a PROM that contains a microprogram, which is used by the disk interface.

DISK DRIVE CONTROL.—The disk drive control provides for the transfer of control

- Selection of the appropriate disk drive

- Selection of the operation to be performed

- Information required to perform the selected operation.

The disk drive control has two registers to store provisional seek information required from the low-speed bus via the disk data processor.

SECTOR LOCATOR.—The sector locator contains the logic to determine when the appropriate sector is positioned beneath the read/write head. When properly positioned, the desired operation (read/write) will be performed. The sector locator will abort an operation if the start of a new sector is encountered before the operation is completed.

DRIVE UNIT INTERFACE.—The drive unit interface provides for the transfer of data and control information between the disk drive and the disk interface via the A and B cables. This transfer ability is under the control of the disk data processor for data transfer and the disk drive control for control signal transfers.

Front Panel Interface

The front panel interface is an independently/interdependently operating computer. It facilitates the man-machine interface occurring at the front panel of the controller. These interface functions provide for the operation, monitoring, and testing of the controller.

The front panel interface (figure 3-68) is divided into the following functional areas:

- Low-speed bus interface

- Microprocessor

- Keyboard logic

- Display logic.

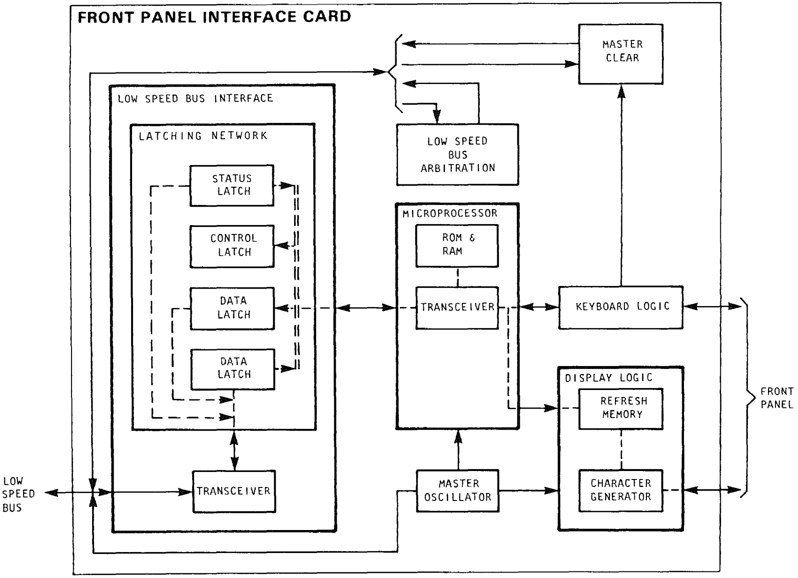

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Figure 3-68.—Front panel interface functional block diagram.

low-speed bus interface provides the ability for the front panel interface to transfer commands, data, and status signals to the appropriate host interface. The elements that enable this ability are a transceiver, two data latches, a control latch, and a status latch.

MICROPROCESSOR.—The microprocessor provides basic control of the front panel interface circuitry and includes transceivers, a RAM, and a ROM. The RAM portion of the microprocessor accomplishes the following:

- Stores all messages sent to and from the host or disk interface
- Is used as a "scratch pad" when needed by the ROM
- Stores all variable information needed by the front panel interface.

The ROM is the permanent storage area for the microprogram used by the front panel interface.

KEYBOARD LOGIC.—The keyboard logic contains the circuitry which accomplishes the following functions:

- Provides the status of the front panel switches and pushbuttons.
- Provides the control signals which illuminate various indicator lamps on the front panel.

DISPLAY LOGIC.—The display logic consists of the following:

- A refresh memory
- Character generator
- Timing circuits used to illuminate the light-emitting diode (LED) display on the front panel.

The output of the display logic is transmitted to the front panel to light each position of the display one column at a time.

takes place. Functionally, the front panel can be divided into the following areas:

- Display
- Controls and indicators

DISPLAY.—The display portion of the front panel enables the controller to communicate certain conditions/situations to the operator. By the lighting of various combinations of the eight LEDs, a total of 64 different characters can be indicated.

CONTROLS AND INDICATORS.—Included as indicators are the HOST COMPUTER ACTIVE, FAULT, and MAINT ENBL (Maintenance Enable). The FAULT and MAINT ENBL lamps are controlled by the front panel microprocessor and the HOST COMPUTER ACTIVE indicator(s) are controlled by the corresponding host interfaces.

The pushbuttons on the front panel are encoded and sent to the microprocessor on the front panel interface card. The switches are used to communicate various operational and maintenance functions to the controller.

The HOST ENABLE switches provide a means of enabling/disabling signals from the host computer(s). The MAINT ENBLE, when in the down position, will disable the pushbutton switches on the "Data" section of the front panel as well as the LED display. The RESET button serves as the unit master clear.

Power Distribution

Primary input power for the Model 3985 disk controller is 115 V ac received via a connector (designated P30) on the rear panel of the unit. Dc operating voltages are then provided by a power-supply assembly, which is located on the rear portion of the controller chassis. The power-supply assembly (figure 3-69) includes a regulated unit that supplies −5 volts at 3 amperes and a separate switching unit to supply +5 volts at 3.5 amperes.

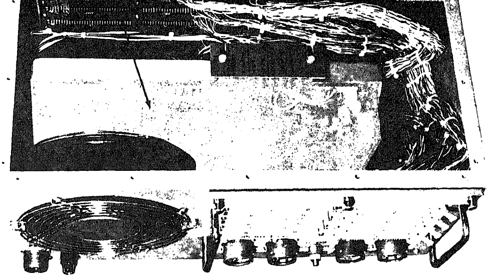

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Figure 3-69.—Power supply with chassis access cover removed.

Controller Cooling System

The disk controller assembly is cooled by an nduced draft system (figure 3-70). This draft ystem is produced by a fan mounted in the rear anel of the controller.

When the controller is operating, air is rawn into the air grill in the front panel, forced ver the circuit cards, and exhausted through an ir grill at the rear of the unit.

CONTROL DATA CORPORATION (CDC) 9766 (MODELS BK6XX AND BK7XX) STORAGE MODULE DRIVE (SMD)

In Part 1 of this module, you were introuced to the description and theory of operation f a generic type of SMD (magnetic disk). (You ill often encounter the short term "disk drive" hen referring to a SMD.) If you are not familiar ith this information, you should again review e applicable portions of Part 1.

Although the following discussion applies to specific type of SMD, you may encounter ther types. The theories and practices that apply to the 9766 SMD can also be applied to other types of disk drive units.

The CDC BK6XX and BK7XX SMDs are high speed, random access digital data storage devices that connect to a host computer through a controller. The major difference between the two drive models is in their data storage capability. The BK6XX can store up to 150 megabytes of data, whereas the BK7XX has twice that capability (300 megabytes).

FUNCTIONAL OVERVIEW

The major functional areas of the drive are illustrated in figure 3-71. In the following paragraphs, we will give a brief overview of these areas.

Disk Pack

The disk pack is the recording medium for the drive. The disk pack consists of 12, 14-inch disks, center-mounted on a hub (figure 3-72). There are 19 recording surfaces and one servo surface. The servo surface contains prerecorded information that is used by the servo circuitry to position the heads at the desired area on the disk

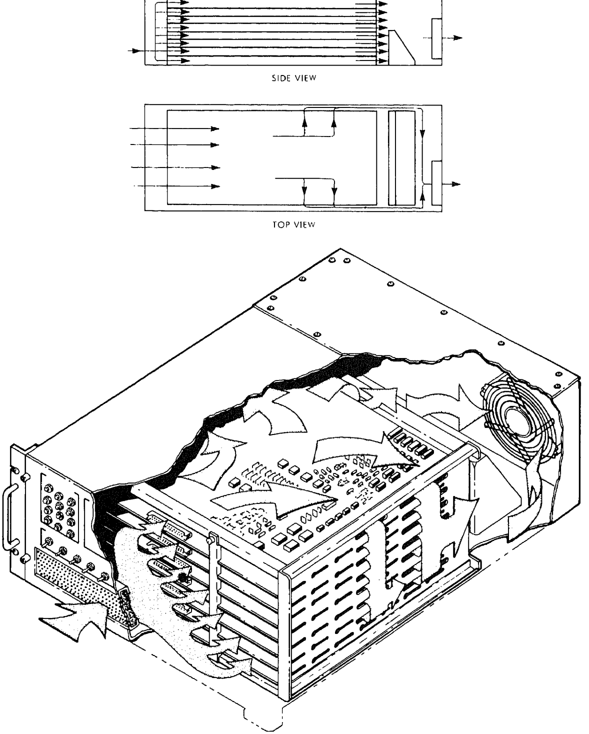

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Figure 3-70.—Controller cooling system.

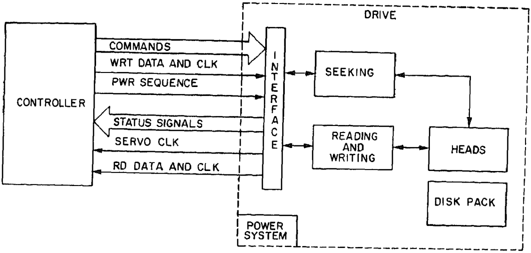

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Figure 3-71.—Drive functional blocks.

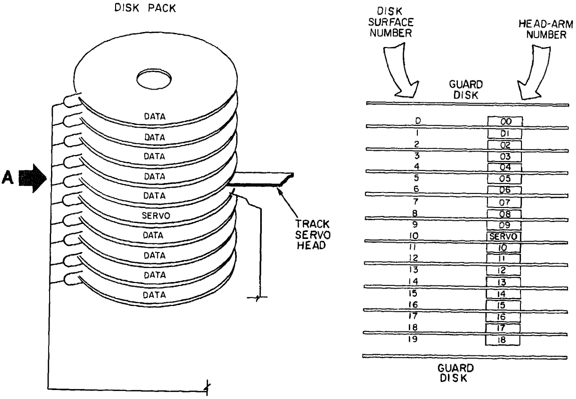

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Figure 3-72.—Disk pack construction.

pack. The top and bottom disks on the pack are for protection only and, therefore do not contain data.

The 19 recording surfaces are used to store data. Each of these recording surfaces has its recording tracks grouped in a 2-inch band near the outer edge of the disk.

The disk pack is portable and is interchangeable between drives. The BK6XX and BK7XX use the same type of disk pack. The track widths of the BK6XX and BK7XX determine the data storage capability. The BK6XX uses .004 inch track width and the BK7XX uses .002 inch track width. There are a maximum of 823 tracks per platter available to the BK7XX with its .002 inch track width. The BK6XX, on the other hand, can use only 411 tracks because of its .004 inch track width. The track width is determined by drive electronics and head configurations—not by the disk pack itself.

Power System

The drive has its own self-contained power supply, which receives its input from the main power source of the site. The power supply provides all the voltages necessary for drive operation.

Interface

The drive cannot communicate directly with the host computer, but must use an interfacing device, called a controller, to accomplish this task. The controller issues all commands to the drive, which decodes these commands and initiates the proper operation. In addition to the commands, the controller sends write data, write clock, and power sequence information to the drive.

The disk drive, on the other hand, sends various status signals, read data, read clock, and servo clock information to the controller. These signals are used by the controller to monitor and control operations performed by the drive.

Seeking

The disk drive must position the heads over the proper portion on the disk pack before it can perform write or read operations. This function, called seeking, is performed by a servo system consisting of control logic and a head-positioning mechanism.

Reading and Writing

The disk drive can write and read data from the disk pack. During a write operation, the drive receives data from the controller, processes it, and writes the data on the disk pack. During a read operation, the drive reads data from the disk pack and transfers this data to the controller.

PHYSICAL DESCRIPTION

The CDC 9766 Models BK6XX and BK7XX can be divided into the following two major areas:

- Storage Module Drive (SMD) Assemblies
- Logic and Circuitry

The following discussion describes the characteristics of these major physical areas.

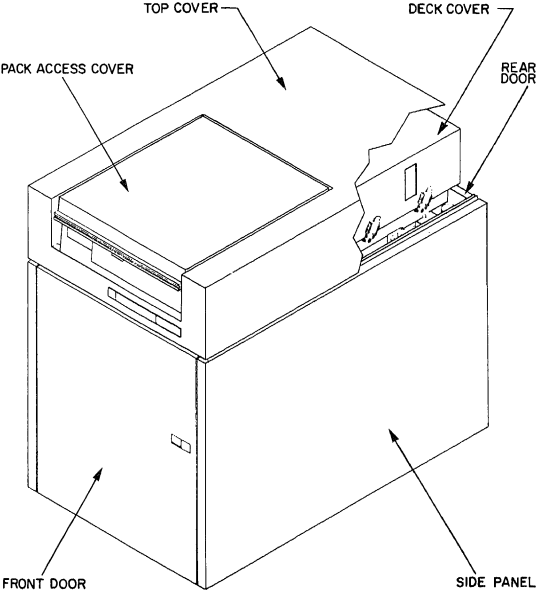
SMD Assemblies

The major SMD assembly elements are shown in figures 3-73 and 3-74. Table 3-8 provides a description of these elements.

SMD Components

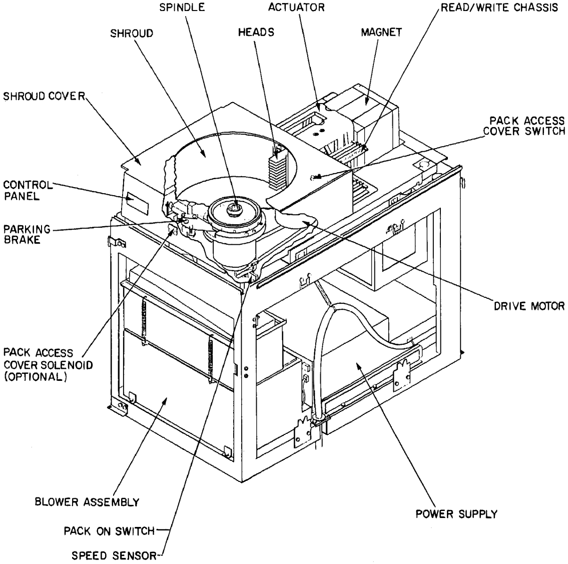
The SMD contains integrated and discrete component circuits. It also contains relays, switches, and other electromechanical elements that enable the SMD to perform its various functions.

Diagrams showing all circuits and interconnecting wiring arrangements can be found in the manufacturers' maintenance manuals.



182.209.2

Figure 3-73.—CDC BK6XX/BK7XX SMD.



182.209.3

Figure 3-74.—BK6XX/BK7XX drive assemblies.

Table 3-8.—Drive assemblies

Actuator	Contains voice coil and carriage. This assembly positions the heads over the disk pack.
Blower Assembly	Contains a blower motor that circulates cooling air for the drive.
Deck Cover	Provides an electrical interference shield for the drive and also reduces noise level output from drive.
Drive Motor	Provides rotational motion that turns spindle and disk pack.
Front Door	Provides access to blower assembly and the lower front part of cabinet.
Heads	Detect data transitions that are on the pack if drive is reading. Writes data transitions on the disk pack if drive is writing.
Logic Chassis	Contains logic cards that control operation of drive.
Magnet	Provides permanent magnetic field that is used in conjunction with voice coil to move carriage and heads.
Operator Control Panel	Contains switches that allow operator to control and monitor basic operation of drive.
Pack Access Cover	Provides access to disk pack and pack area.
Pack Access Cover Solenoid (Optional)	Prevents pack access cover from being opened if the pack is spinning.
Pack Access Cover Switch	Interlock that de-energizes drive motor if pack access cover is opened while pack is spinning. It also prevents motor from starting unless cover is closed.
Pack On Switch	Interlock that prevents drive motor from starting when pack is not installed.
Parking Brake	Holds spindle while disk pack is being installed and removed.
Power Supply	Furnishes all necessary voltages for drive operation.
Read/Write Chassis	Contains cards that are essential to drive read/write operations.
Rear Door	Provides access to power supply, logic chassis and lower rear of cabinet.
Shroud and Shroud Cover	Provides protection and ventiliation for disk pack.
Side Panels	Provide access to either side of drive.
Spindle and Lockshaft-	Provides mounting surface for disk pack. Lockshaft secures disk pack to spindle. Drive motor transmits rotational motion to spindle via drive belt thereby causing disk pack to rotate.
Top Cover	Covers entire top of drive thereby protecting drive assemblies and reducing output noise level.

182.209.4

associated with the SMD can be determined by the equipment identification plate and the Field Change Order (FCO) log. To determine if the maintenance manuals and procedures being used apply to the SMD on which you are working, you must know the configuration of the SMD. The following discussion will enable you to determine and analyze the information entered on the equipment identification plate, FCO log, and the maintenance manual to equipment correlation.

Equipment Identification Plate

The manufacturer attaches the equipment identification plate (figure 3-75) to the drive frame at the rear of the unit when it leaves the factory. This plate identifies the basic mechanical and logical configuration of the disk drive. The [illegible]. The equipment identification [illegible] divided into two parts as shown by following example:

BK6 A2A
Equipment Identifier Type Identifier

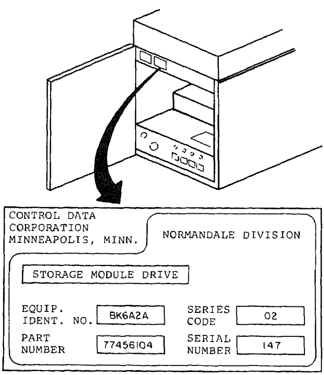
Equipment Identifier.—The equipment identifier indicates the basic functional capabilities of the drive. This number will be either BK6 or BK7.

Type Identifier.—The type identifier identifies variations in drives that have the same equipment identifier.

Equipment variations are installed to adapt a drive to a specific system requirement. However, these variations do not alter the overall capability of the drive. The variations adapt a particular SMD for a variety of voltage requirements and standard options. The standard options are those features installed when the drive leaves the factory. A configuration chart (table 3-9) lists input voltage requirements and standard options for all types of BK6 and BK7 drives. The standard options listed in this chart are as follows:

- A Cable I/O—Drive A cable connector may have 50, 60, or 75 pins.
- Dual channel—Allows the drive to be connected to two controllers (one drive may be shared by two different host computers).
- Index and sector configuration—Enables signals associated with the index and sector selection to be carried on the A cable, B cable, or both.
- Pack access cover solenoid—Solenoid that locks the pack access cover in the closed position while the park is spinning.
- Color code—When used with the equipment configuration chart and the parts list (from maintenance manual), helps provide the eight-digit number needed to order parts for all SMD units.

SERIES CODE.—The series code represents when a unit was built. While all units are interchangeable at the system level, regardless of series



CONTROL DATA CORPORATION MINNEAPOLIS, MINN.
NORMANDALE DIVISION
STORAGE MODULE DRIVE
EQUIP. IDENT. NO. BK6A2A
SERIES CODE 02
PART NUMBER 77456104
SERIAL NUMBER 147

182.209.5
Figure 3-75.—Equipment identification plate.

	VOLTAGE		OPTIONS					
EQUIPMENT	208 v 60 Hz	220 v 50 Hz	A Cable I/O	Dual Channel	Index & Sector Configuration	Pack Access Cover Solenoid	TLA* Number	Color Code
BK6A1A	X		60-pin		S&IOAC		77456102	A
BK6A1B		X	60-pin		S&IOAC		77456103	A
BK6A1D		X	60-pin		S&IOAC		77456120	G
BK6A1E	X		60-pin		S&IOBC		77456121	L
BK6A1F		X	60-pin		S&IOBC		77456122	L
BK6A1G	X		60-pin		S&IOAC		77456125	S
BK6A1H		X	60-pin		S&IOAC		77456126	S
BK6A2A	X		60-pin	Yes	S&IOAC		77456104	A
BK7A1K		X	60-pin		S&IOBC	Yes	77456034	K
BK7A1L	X		60-pin		S&IOAC		77456037	△1
BK7A1M		X	60-pin		S&IOAC		77456038	△1
BK7A1N	X		60-pin		S&IOBC		77456039	L
BK7A1P		X	60-pin		S&IOBC		77456040	L
BK7A1R	X		60-pin		S&IOAC		77456043	M
BK7A1S		X	60-pin		S&IOAC		77456045	M
BK7A1T	X		60-pin		S&IOAC		77456046	N

* For factory use only.

** Defined under Equipment Configuration in section 1 of this manual.

*** 208 Volt, 60 Hz drives can be rewired for 230 Volt, 60 Hz and 220 Volt, 50 Hz drives can be rewired for 240 Volt, 50 Hz. See Installation Section in Maintenance Manual.

△1 Unit has Special Manual Supplement.

182.209.6

code, part differences may exist with units having different series codes. When a part difference exists, that difference is noted in the parts data section of the hardware maintenance manual.

PART NUMBER.—The part number is for factory use only.

SERIAL NUMBER.—Each drive has its own serial number assigned. Serial numbers are sequentially assigned within a family of drives. Therefore, no two equipments will have the same serial number.

FCO Log

Field Change Orders (FCOs) are electrical or mechanical changes that may be performed at he factory or in the field. FCOs do not affect he series code. FCOs are indicated by an entry on the FCO log that accompanies each machine. The components of a machine with an FCO installed may not be interchangeable with those of a machine without the FCO. Therefore, it is very important that the FCO log be kept current and consulted before maintenance is performed.

Manual to Equipment Correlation

Throughout the life of a machine, changes are made either in the factory configuration (series code change) or by FCOs. These changes are also reflected in documented changes to the maintenance manual (remember the importance of keeping the FCO log current). To ensure that the maintenance manual correlates to the machine, you should refer to the manual-to-equipment correlation sheet that is located in the front of the maintenance manual. This sheet records all the FCOs that are reflected in the

Logical Address Plug	Determine logical address of drive. Address can be set any number from 0 to 15 by installing the proper plug. If no plug is installed the address is 15. Drive comes from the factory with complete set of logical address plugs each having a unique address. The available plugs with their associated address and part number are listed in the parts data section of the hardware maintenance manual.
START Switch/ Indicator	Pressing button when drive is in power off condition (disk pack not spinning) lights indicator and starts power on sequence, provided the following conditions are met. • Disk pack is installed. • Pack access cover is closed. • All power supply circuit breakers are on. Pressing the indicator when drive is in power on condition (disk pack spinning), extinguishes indicator and starts power off sequence.
READY Indicator	Lights when unit is up to speed, the heads are loaded and no fault condition exists.
FAULT Switch/Indicator	Lights if a fault condition exists within the drive. It is extinguished by any of the following providing reason for fault is no longer present: • Pressing FAULT switch on operator control panel • Fault Clear signal from controller • Maintenance Fault Clear switch on fault card in logic chassis location A17. Conditions causing fault are described in the discussion on Fault Detection in section 3 of this manual.
WRITE PROTECT Switch/Indicator	Pressing switch to light indicator disables the driver write circuits and prevents it from writing data on the pack. Pressing the switch to extinguish the indicator removes the disable from the write circuits.

182.209.8

manual. It should correlate to the machine FCO log if all the FCOs have been installed in the machine and the FCO log has been maintained properly.

CONTROLS AND INDICATORS

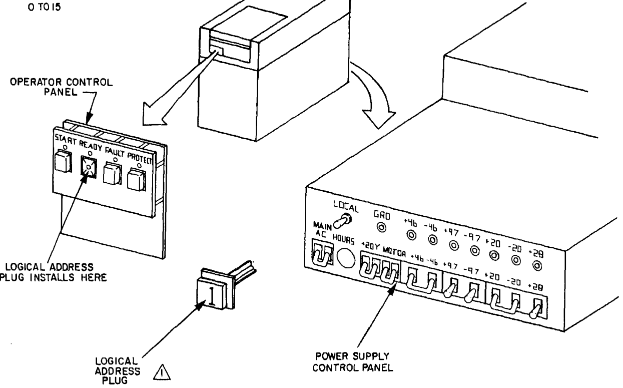
The SMD has two types of controls and indicators used in routine operation of the drive. These controls and indicators are grouped into two areas: the operator control panel and the power supply control panel.

Operator Control Panel

The operator control panel contains switches and indicators used to control and monitor the basic operation of the drive. Figure 3-76 shows the layout of the operators control panel. Table 3-10 describes the functions of these controls and indicators.

Power Supply Control Panel

The power supply control panel switches and indicators provide for the means of controlling and monitoring the operation of the power supply. The power supply control panel contains circuit breakers, test points, and a time meter. The panel can be accessed by opening the rear door of the drive cabinet. Figure 3-76 illustrates the layout of the power supply control panel. Table 3-11 defines the functions of the switches



182.209.7

Figure 3-76.—Controls and indicators.

Table 3-11.—Power supply control panel functions

Control or Indicator	Function
MAIN AC Circuit breaker	Controls application of site AC power to drive. Closing this breaker applies power elapsed time meter.
HOURS Elapsed time meter	Records accumulated AC power on time. Meter starts when MAIN AC circuit breaker is closed.
LOCAL/REMOTE Switch	Controls whether drive can be powered up from drive (LOCAL) or controller (REMOTE). In LOCAL position, drive power on sequence starts when START switch is pressed. In REMOTE position, drive power on sequence starts when START switch is pressed and sequence power ground is received from controller.
+20Y, MOTOR, +46, -46, +9.7, -9.7, +20, -20, +28	Controls application of associated voltages to drive and also provides overload protection.

182.209.9

OPERATING INSTRUCTIONS

Actual operating procedures of the 9766 Models BK6XX and BK7XX vary, depending on site peculiarities and equipment configurations. Therefore, we will not give a detailed discussion of these procedures in this module. You should consult the operators instructions at your particular site for this information.

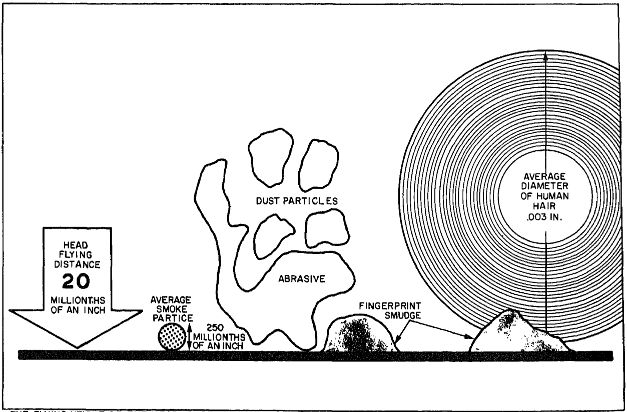
However, one critical area that is essentially the same for all sites is the handling and storage of the disk pack itself. It must be emphasized that the read/write heads do not contact the surfaces of the disk platters in any way. The heads actually "fly" on a thin cushion of air and are separated from the surfaces of the pack by only approximately 20 millionths of an inch.

possibly damage the heads also. You can therefore easily see the importance of the information that follows. Figure 3-77 illustrates the very close proximity of the heads in relation to the disk pack recording surfaces.

Disk Pack Storage

To ensure maximum disk pack life and reliability, you should observe the following procedures:

- When disk packs are installed in the drive, ac power to the SMD should not be secured. If ac power must be secured, you should ensure that any dust that may accumulate inside the pack area is purged before the heads are allowed to be reloaded.



THE FLYING HEIGHT OF THE HEAD IS 150 TIMES SMALLER THAN A HUMAN HAIR.

182.210

Figure 3-77.—Illustration of head flying distance.

° F to 90° F and the relative humidity should 10 percent to 80 percent.

- If the disk pack must be stored in a ferent environment, allow 2 hours of adjustnt to machine-room environment before use.

- Never store the disk pack in direct sunıt or in a dirty environment.

- Store disk packs flat, not on edge. They y be stacked (flat) with similar packs when red.

- Always be sure that both top and bottom stic covers are on the disk pack and are securely ked together when the disk pack is not actually talled in the drive.

- Do not attach any label to the disk pack elf. Labels will not remain attached when the ck is spinning and severe head damage may ult. Any labels, if attached, are to be affixed the pack canister.

- Cleaning of pack surfaces is not recomnded.

you with an introductory overview of the theory of operation of the BK6XX and BK7XX SMDs. These operational theories will include a description of various drive operations and the hardware used in performing these operations. We will examine the following major areas (refer to figure 3-78):

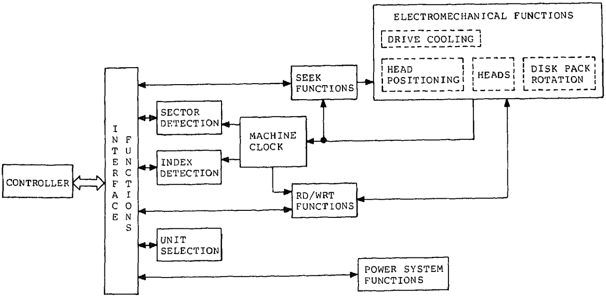
- Power system functions—Describes how the drive provides the voltage necessary for drive operation.

- Electromechanical functions—Provides a physical and functional description of the mechanical and electromechanical portions of the disk pack rotation, head positioning, and air flow system of the drive.

- Interface functions describes the signal lines connecting the drive and controller.

- Unit selection—Describes how the controller logically selects the drive so the drive will respond to controller commands.

- Seek functions—Describes the function of the head positioning mechanism in positioning the head over the disk pack.



182.209.10

Figure 3-78.—Drive functional block diagram.

- Index function—Describes the process of locating the index pattern, which is used to indicate the logical beginning of each track.

- Sector detection—Describes the use of sector pulses which are used to determine the angular position of the index in respect to the read/write heads.

- Head selection—Describes the head selection process.

- Read/write functions—Describes the reading and writing of data.

- Fault detection—Describes the conditions that the drive circuitry will interpret as a fault.

As we mentioned earlier, the following discussion is of an introductory nature only. You can obtain more specific information from the manufacturers technical manuals.

Power Supply Functions

The major element in the power system of the SMD is the power supply assembly (figure 3-78). The power supply derives its input from the site ac power source. The ac power is then processed by the power supply, which provide all the dc and ac voltages necessary for drive operation. These voltages are distributed to the drive circuit breakers located on the power supply. The circuit breakers also provide overload protection.

Site ac power is inputted to the power supply via the MAIN AC circuit breaker. When this circuit breaker is closed, power is also supplied to the hour meter and the drive motor control triacs. However, the motor will not start rotating until the power on sequence is initiated (see START SWITCH indicator under operating instructions).

The drive motor is started and the heads load function is initiated during the power on at the controller (REMOTE).

Electromechanical Functions

Certain drive functions are a result of the electromechanical devices working under the control of logic circuitry. These functions include:

- Disk pack rotation

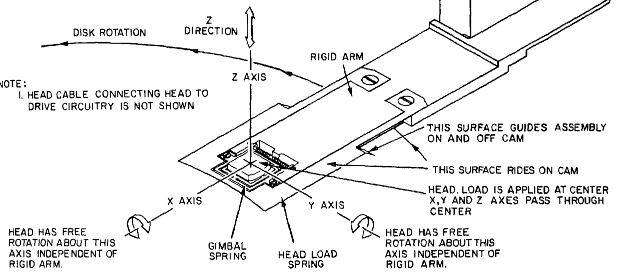
- Head positioning

- Drive cooling and ventilation.

DISK PACK ROTATION.—Disk pack rotation is performed by the disk pack rotation mechanism, which is controlled by the power system. In part this consists of an ac motor and associated circuitry. The purpose of the disk pack rotation is to create a cushion of air on the disk surfaces. This cushion of air allows the heads to move (fly) over the disk surfaces without actually contacting them. The disk pack must be rotating fast enough to allow the heads to fly before any load operations can be performed. As we mentioned earlier in our discussion, nominal speed of the disk pack during normal operation is about 3600 rpm.

HEAD POSITIONING.—The heads are electromagnetic devices that record data and/or read it from the disk pack. The heads and the support arm on which they are mounted are called a head-arm assembly (figure 3-79). The drive has 20 heads; 19 read/write heads and 1 read head, which is used to read information from the servo surface.

The heads must be loaded before they can be positioned to a data track for the recording and reading of data. Loading the heads consists of moving the heads forward from their retracted (unloaded) position until they are over the disk surface. All heads are loaded at the same time. The load sequence is initiated during the power up sequence when the disk pack has reached about 3000 rpm.


DISK ROTATION
Z DIRECTION
Z AXIS
RIGID ARM
OTE:
I. HEAD CABLE CONNECTING HEAD TO DRIVE CIRCUITRY IS NOT SHOWN
THIS SURFACE GUIDES ASSEMBLY ON AND OFF CAM
THIS SURFACE RIDES ON CAM
HEAD. LOAD IS APPLIED AT CENTER X,Y AND Z AXES PASS THROUGH CENTER
X AXIS
Y AXIS
HEAD HAS FREE ROTATION ABOUT THIS AXIS INDEPENDENT OF RIGID ARM.
GIMBAL SPRING
HEAD LOAD SPRING
HEAD HAS FREE ROTATION ABOUT THIS AXIS INDEPENDENT OF RIGID ARM.

182.209.11

Figure 3-79.—Head-arm assembly.

As we discussed previously, the heads do not ntact the disk surface but actually "fly" on a shion of air. If a situation develops that could nceivably cause the heads to contact the disk rface, the head position mechanisms and logic ll cause an emergency retract to take place. at is, the heads are repositioned at their racted position at a very high rate of speed. ie such condition that will cause this to take ice is a loss of disk pack speed. The emergency ract sequence will be initiated if the speed of spindle motor, which drives the disk pack, ops below 2700 rpm. Sensors are also available at will detect a condition which could cause a s of disk pack speed. These conditions lude:

- Loss of ac power—If site ac power is lost, dc power is also lost. This condition will use emergency retract.
- Loss of +20, −16, or +9.7 V dc will use emergency retract.

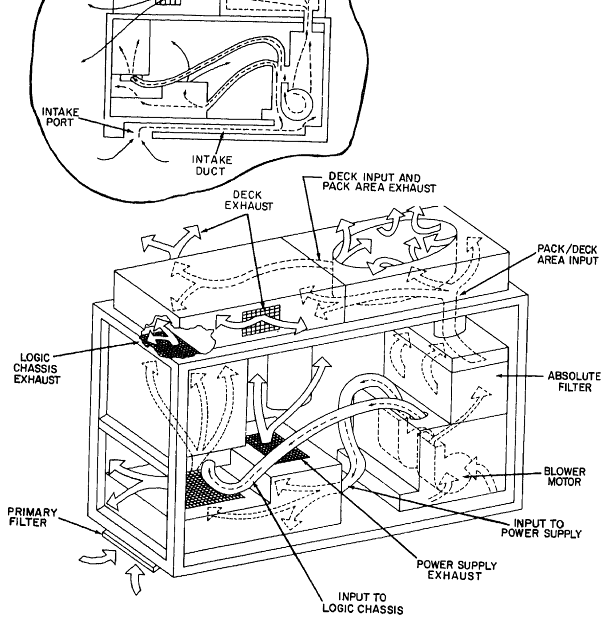
DRIVE COOLING AND VENTILATION.— e air flow system (figure 3-80) provides ntilation and cooling air for the drive.

The blower assembly is the heart of the air flow system. This assembly consists of the blower motor, absolute filter, input port from the primary filter and output ports to the logic chassis, power supply, and disk pack area.

The blower motor provides the pressure needed to draw air into and push it through the system. The system intake port is located under the rear of the cabinet. This port is covered by the primary filter, which prevents large foreign particles from being drawn into the system. Air flows from the intake port through a duct in the floor of the cabinet to the blower motor.

The blower motor forces air to the power supply, logic chassis, pack area and deck areas. The air to the logic chassis and power supply, flows through hoses connected between these assemblies and the blower assembly. The air exhausted by the power supply and logic chassis circulates through the lower part of the drive cabinet and provides cooling air for the spindle motor.

The air to the pack area is filtered by the absolute filter, which removes particles that



182.209.12

Figure 3-80.—Air flow system.

might cause damage to the pack or heads. The air is forced into the pack area from all sides, causing a positive pressure. This results in an upward dispersion of air, thus preventing the entrance of contaminated air through the pack access cover.

The air intake for the pack area is also forced into the deck area through vents in the rear of the shroud. This air cools the deck components and exits through vents on each side of the deck cover.

controller must pass through the interface. SMD comes from the factory as either a gle- or dual-channel unit (sometimes referred as ports). Single-channel units can connect and communicate with one controller: dual-nnel units can accommodate two controllers. e interface in both cases consists of the I/O les (designated as A and B cables) and logic uired to carry and process the signals sent ween the SMD and controller. Figure 3-81 strates the single- and dual-channel interface nfigurations.

it Selection

For an SMD to respond to commands from controller, the SMD must receive a "select" nal from the controller (multiple SMDs may attached to a single controller). In both gle- and dual-channel units the select sequence nitiated by a unit select tag signal from the ntroller. The specific sequences performed by SMDs after receipt of the unit select tag somewhat different between the single- and al-channel units. The reason for this is that dual channel units must solve the problem of o controllers trying to select the drive when ly one can have it at any one time.

the heads over the desired cylinder on the disk pack. The servo circuits of the SMD control this function.

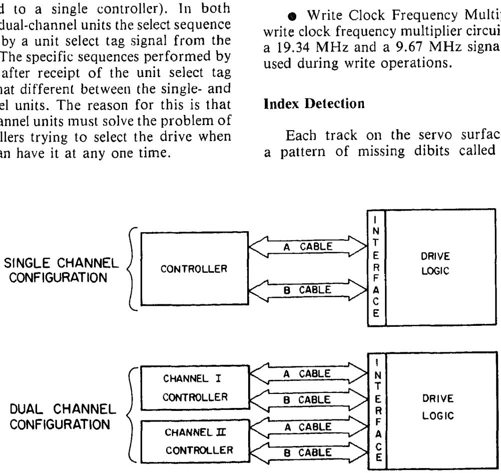
Machine Clock

The machine clock circuits generate the clock signals necessary for SMD operation. These circuits are divided into two areas:

- Servo Clock Multiplier—These circuits generate clock pulses used by the sector detector, index detection and the read phase lock oscillator (PLO) circuits. These circuits also generate the 9.67 MHz servo clock signal that is sent to the controller.
- Write Clock Frequency Multiplier—The write clock frequency multiplier circuit generates a 19.34 MHz and a 9.67 MHz signal, which is used during write operations.

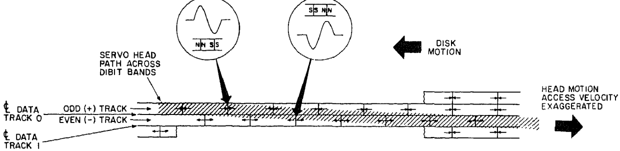
Index Detection

Each track on the servo surface contains a pattern of missing dibits called the index



182.209.13

Figure 3-81.—Single/dual channel configurations.



182.209.14

Figure 3-82.—Positive/negative dibits.

pattern. Dibits (a shortened term for dipolar bit) are recorded on the servo surface during manufacture. Dibits are the result of the manner in which flux reversals are recorded on the servo tracks (figure 3-82). One type of track, known as the even track, contains negative dibits. The other track, the odd track, contains positive dibits. When the index detection circuits of the SMD detect this pattern, a 2.5 μsec index signal is generated. This indicates to the SMD and its controller the logical beginning of a track.

Sector Detection

The sector detection circuits generate signals that are used by the SMD electronic circuits to determine the angular position of the heads with respect to the index pattern. These signals are referred to as sector pulses. A specific number of these pulses are generated during each revolution of the disk pack. The sector pulses logically divide the disk pack recording surfaces into areas called sectors.

Head Selection

A specific read/write head must be selected before a read write operation can be performed (remember that there are 19 possible read/write heads). Head selection is initiated when the controller sends the SMD a head select tag and a head address. This signals the head current driver associated with the selected head, which allows the head to perform the desired operation.

Read/Write Functions

When the SMD is on cylinder and the proper head has been selected, a read or write operation can be performed. The controller initiates a read or write operation by sending the SMD a control tag and the proper bit patterns.

During a read operation, the drive recovers data from the disk and transfers it to the controller. During a write operation, the SMD receives data from the controller and records it on the disk pack.

Fault and Error Conditions

The errors that the SMD can detect as error conditions can be divided into two categories:

- Those indicated by the fault latch and register
- Those not indicated by the fault latch and register.

Only those conditions indicated by the fault latch and register will be examined in the following discussion. Specific details of the error conditions, which are not indicated by the fault latch and register, can be obtained from the manufacturers technical manuals.

ERRORS INDICATED BY FAULT LATCH REGISTER.—Certain error conditions will set the fault latch of the SMD and also set the fault register latches associated with the error

- Enables the fault line to the controller

- Lights the fault indicator on the operator panel (SMD)

- Clears the unit ready signal of the drive

- Inhibits the write and load circuitry of the drive.

The occurrence of these events prevents rther drive operations from being performed itil the error is corrected and the fault latch is eared.

If the error condition has been corrected, the ult latch can be cleared by any of the following ethods:

- Activating the FAULT switch on the operator panel

- Controller FAULT CLEAR signal from the controller

- Activating the MAINTENANCE FAULT CLEAR switch on Fault Card

- Power-down the SMD.

When an error occurs that causes the fault tch to go to a set state, a latch in the fault gister is also set. These latches provide a eans of storing the error indication so that it n be referenced at a later time for maintenance irposes. The fault register latches can be eared by powering down the SMD or by tivating the FAULT CLEAR switch on the ult card.

The following discussion identifies and scribes the conditions that will cause the fault tch and fault register latches to be set.

WRITE FAULT.—A write fault will occur if y of the following conditions exist:

- Low voltage output from the write driver

- Low current input to the write driver

- Low +22 volt input to write driver

MORE THAN ONE HEAD SELECTED.—The more-than-one-head-selected fault is generated when more than one read/write head is selected. If more than one head is selected, the monitoring circuitry will generate a multiple select fault.

READ AND WRITE.—The read and write fault is generated when a read and write gate occur simultaneously.

OFF CYLINDER.—The off-cylinder fault is generated if the SMD is in an off cylinder condition and it receives a read or write gate from the controller.

VOLTAGE FAULT.—The voltage fault is generated when the ±46, ±5, or ±20 voltages are below satisfactory operating levels.

SUMMARY

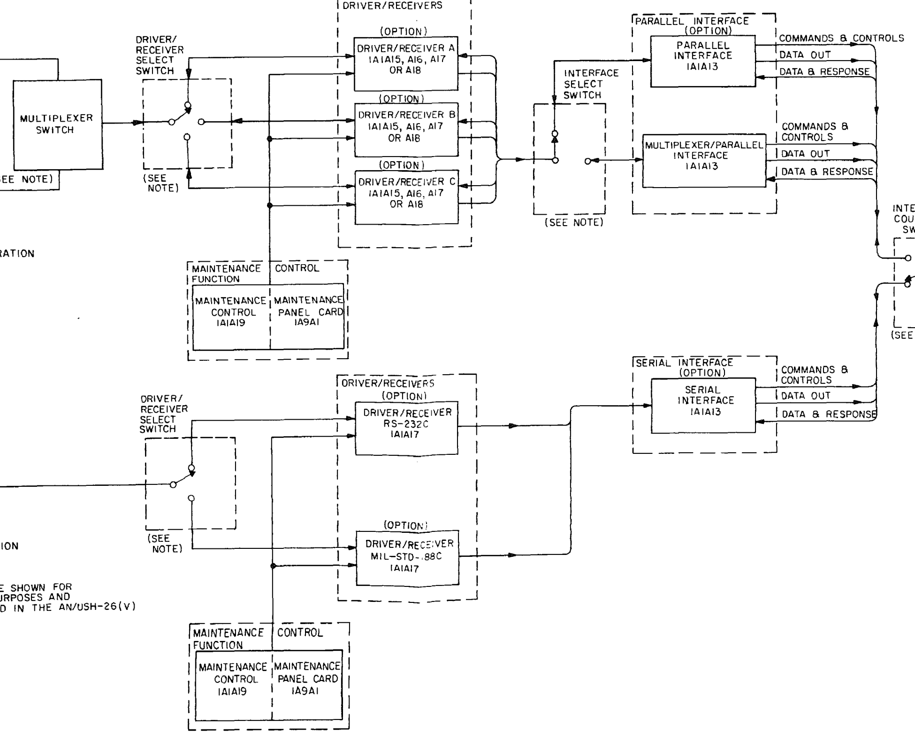
The electronic equipments within the Ocean Systems community are constantly being refined and updated and represent the latest technologies. This module introduced you to the theories and practices you will need to begin building your technical expertise as a maintenance technician. In Part 1 of this module we reviewed the evolution of computers and computing devices and provided a comprehensive look at the hardware units and theories of a modern digital computer.

Part 2 introduced you to some specific computer and processor units, which include the AN/UYK-20, the SDP, and the AN/UYK-7.

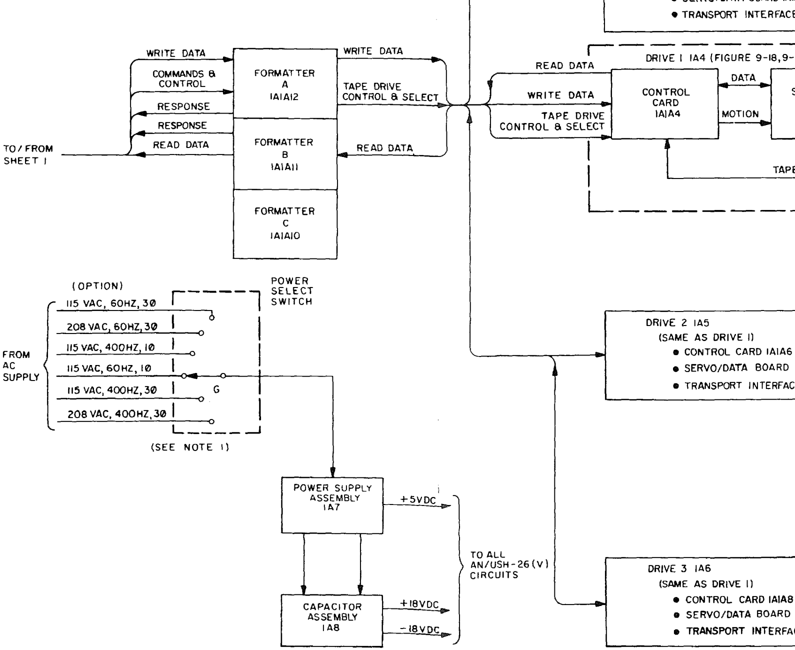
Part 3 provided you with information on the equipments that enable a computer to communicate with the outside world—the peripherals. The MMI devices introduced in Part 3 are very important, for without their existence the processing ability of a computer would be virtually useless.

The equipments covered in this module represent the basic items that you will encounter within the Ocean Systems community. Although other varieties of equipments exist, the knowledge you gained from this module will prove invaluable in helping you learn the maintenance practices on other equipment. You must keep in mind tainer), are a critical link in the operational

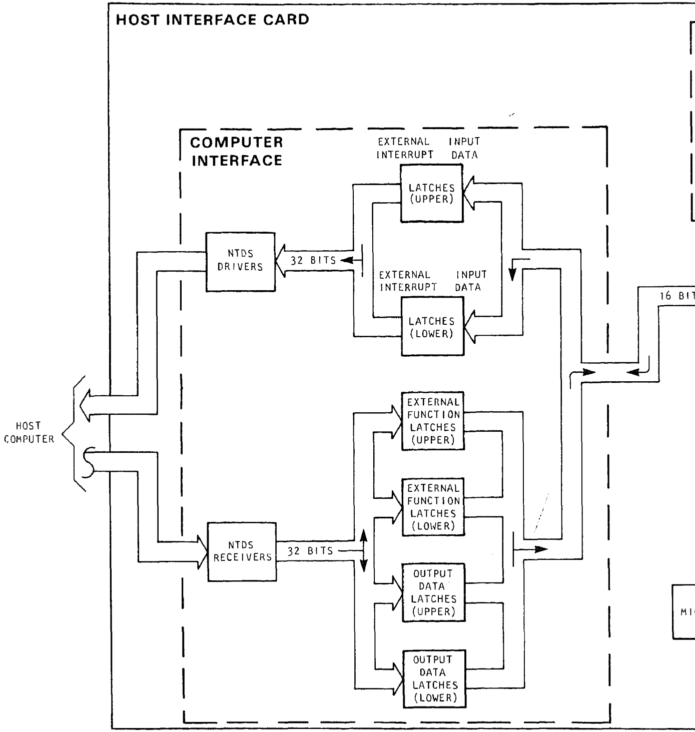
ensure this does not happen.



MULTIPLEXER SWITCH
EE NOTE)
RATION
DRIVER/ RECEIVER SELECT SWITCH
(SEE NOTE)
DRIVER/RECEIVERS
(OPTION)
DRIVER/RECEIVER A 1A1A15, A16, A17 OR A18
(OPTION)
DRIVER/RECEIVER B 1A1A15, A16, A17 OR A18
(OPTION)
DRIVER/RECEIVER C 1A1A15, A16, A17 OR A18
MAINTENANCE FUNCTION
CONTROL
MAINTENANCE CONTROL 1A1A19
MAINTENANCE PANEL CARD 1A9A1
INTERFACE SELECT SWITCH
(SEE NOTE)
PARALLEL INTERFACE (OPTION)
PARALLEL INTERFACE 1A1A13
COMMANDS & CONTROLS
DATA OUT
DATA & RESPONSE
MULTIPLEXER/PARALLEL INTERFACE 1A1A13
COMMANDS & CONTROLS
DATA OUT
DATA & RESPONSE
INTE
COU
SW
(SEE
DRIVER/ RECEIVER SELECT SWITCH
(SEE NOTE)
ION
E SHOWN FOR
URPOSES AND
D IN THE AN/USH-26(V)
DRIVER/RECEIVERS (OPTION)
DRIVER/RECEIVER RS-232C 1A1A17
(OPTION)
DRIVER/RECEIVER MIL-STD-188C 1A1A17
MAINTENANCE FUNCTION
CONTROL
MAINTENANCE CONTROL 1A1A19
MAINTENANCE PANEL CARD 1A9A1
SERIAL INTERFACE (OPTION)
SERIAL INTERFACE 1A1A13
COMMANDS & CONTROLS
DATA OUT
DATA & RESPONSE



Foldout 3-1.—Overall functional block di


HOST INTERFACE CARD
COMPUTER INTERFACE
EXTERNAL INTERRUPT
INPUT DATA
LATCHES (UPPER)
NTDS DRIVERS
32 BITS
EXTERNAL INTERRUPT
INPUT DATA
LATCHES (LOWER)
16 BIT
HOST COMPUTER
EXTERNAL FUNCTION LATCHES (UPPER)
EXTERNAL FUNCTION LATCHES (LOWER)
NTDS RECEIVERS
32 BITS
OUTPUT DATA LATCHES (UPPER)
OUTPUT DATA LATCHES (LOWER)
MI

GLOSSARY AND LIST OF TERMS COMMONLY USED IN MANUFACTURERS' TECHNICAL MANUALS

ABSOLUTE ADDRESS.—An address permanently assigned by the machine designer to a storage location. Same as machine address, specific address.

ABSOLUTE CODING.—Coding that uses machine instructions with absolute addresses.

ABSOLUTE ERROR.—(1) The amount of error expressed in the same units as the quantity containing the error. (2) Loosely, the absolute value of the error, that is, the magnitude of the error without regard to its algebraic sign.

ABSOLUTE INSTRUCTION.—A machine instruction in its final executable form.

ACCEPTOR.—An impurity that can make a semiconductor a P-type by accepting valence electrons, thereby leaving "holes" in the valence band. The holes act as carriers of a positive charge.

ACCESS ARM.—A part of a disk storage unit that is used to hold one or more reading and writing heads.

ACCESS TIME.—(1) The time interval between the instant at which data is called for from a storage device and the instant delivery begins. (2) The time interval between the instant at which data is requested to be stored and the instant at which storage is started.

ACCUMULATOR.—A register in which the result of an arithmetic or logic operation is formed.

ADAPTER.—A device used to effect operative capability between different parts of one or more systems or subsystems.

ADDER.—A device whose output is a representation of the sum of the quantities represented by its inputs.

ADDRESS.—(1) An identification, as represented by a name, label, or number, for a register, location in storage, or any other data source or destination, such as the location of a station in a communications network. (2) Loosely, any part of an instruction that specifies the location of an operand for the instruction.

ADDRESS PART.—A part of an instruction word that specifies the address of an operand, instruction, or result.

ADDRESS REGISTER.—A register in which an address is stored.

ADDRESSING MODES.—An address is a coded instruction designating the location of data or program segments in storage. The address may refer to storage in registers or memories or both. The address code may be stored so that a location may contain the address of data rather than the data itself. This form of addressing is common in microprocessors. Addressing modes vary considerably because of efforts to reduce program execution time.

ALGOL.—(ALGOrithmic Language). A language primarily used to express computer programs by algorithms.

ALGORITHM.—A prescribed set of well-defined rules or processes for the solution of a problem in a finite number of steps; for example, a full statement of an arithmetic procedure for evaluating sin x to a stated precision.

ALGORITHMIC LANGUAGE.—A language designed for expressing alogrithms.

ALLOYED JUNCTION.—A PN junction formed by recrystallization of a molten region of P-type material on an N-type substrate, or vice versa.

acter set containing letters, digits, and usually other characters, such as punctuation marks.

ALPHANUMERIC CHARACTER SET.—A character set containing letters, digits, and usually other characters.

ALPHANUMERIC CODE.—A code whose code set consists of letters, digits, and associated special characters.

ALTERNATION.—One-half of a complete cycle.

ALU.—(ARITHMETIC AND LOGIC UNIT). The ALU is one of the three essential components of the central processing unit of a computer. The other two are the internal data storage unit and the control unit. The ALU performs various forms of addition and subtraction; the logic mode performs such logic operations as ANDing the contents of two registers or masking the contents of a register.

AMMETER.—An instrument for measuring the amount of electron flow in amperes.

AMPERE.—The basic unit of electrical current.

AMPERE-TURN.—The magnetizing force produced by a current of one ampere flowing through a coil of one turn.

AMPLIFICATION.—The process of increasing the strength (current, power, or voltage) of a signal.

AMPLIFIER.—A device used to increase the signal voltage, current, or power. It is generally composed of a vacuum tube or transistor and associated circuitry (collectively referred to as a stage). An amplifier may contain several stages to obtain a desired gain.

AMPLITUDE.—The maximum instantaneous value of an alternating voltage or current, measured in either the positive or negative direction.

harmonic distortion.

ANALOG.—Pertaining to representation by means of continuously variable physical quantities.

ANALOG COMPUTER.—(1) A computer in which analog representation of data is mainly used. (2) A computer that operates on analog data by performing physical processes on these data.

AND.—A logic operator having the property that if P is a statement, Q is a statement, R is a statement,..., then the AND of P, Q, R,... is true if all statements are true, false if any statement is false. P AND Q is often represented by $P \cdot Q$, PQ. Synonymous with logical multiply.

AND GATE.—A gate that implements the logic AND operator.

ANODE.—A positive electrode; the plate of a vacuum tube.

AQUADAG.—A graphite coating on the inside of certain cathode-ray tubes for collecting secondary electrons emitted by the screen.

ARITHMETIC SHIFT.—(1) A shift that does not affect the sign position. (2) A shift that is equivalent to the multiplication of a number by a positive or negative integral power of the radix.

ARITHMETIC UNIT.—The unit of a computing system that contains the circuits that perform arithmetic operations.

ARMATURE.—(1) The rotating part of a dc electric motor or generator. (2) The moving part of a relay or vibrator.

ASCII.—American Standard Code for Information Interchange. The standard code, using a coded character set consisting of 7 bit-coded characters (8 bits with parity), used for information interchange among data processing systems, communications systems, and associated equipment.

for symbolic operation codes and absolute or relocatable addresses for symbolic addresses.

ASSEMBLER.—A program that prepares a program in machine language from a program in symbolic language by substituting absolute operation codes for symbolic operation codes and absolute or relocatable addresses for symbolic addresses.

ASSEMBLY LANGUAGE.—A computer-oriented language, the instructions of which are usually in one-to-one correspondence with computer instructions.

ASSOCIATIVE STORAGE.—A storage device in which storage locations are identified by their contents—not by names or positions.

ASYNCHRONOUS.—Pertaining to a lack of time coincidence in a set of repeated events where this term is applied to a computer to indicate that the execution of one operation is dependent on a signal that the previous operation is completed.

ASYNCHRONOUS COMPUTER.—A computer in which each event or the performance of each operation starts as a result of a signal generated by the completion of the previous event or operation, or by the availability of the parts of the computer required for the next event or operation.

ATTENUATION.—The reduction in the strength of a signal.

AUTOMATIC GAIN CONTROL (AGC).—A method of automatically regulating the gain of a receiver so that the output tends to remain constant though the incoming signal may vary in strength.

AUTOMATIC VOLUME CONTROL (AVC).—See AUTOMATIC GAIN CONTROL.

AUXILIARY OPERATION.—An off-line operation performed by equipment not under control of the central processing unit.

AUXILIARY OPERATION.—An off-line operation performed by equipment not under control of the central processing unit.

AVALANCHE DIODE.—A diode that conducts current only above a certain "breakdown" voltage by virtue of high-field impact ionization (avalanche). Useful for voltage-limiting or microwave generation. (See AVALANCHE MULTIPLICATION and IMPATT DIODE.)

AVALANCHE MULTIPLICATION.—A high-field effect in semiconductors that leads to an increase in current. High-energy charge carriers create additional carriers by impact ionization of valence electrons. (See IMPATT DIODE.)

BAND OF FREQUENCIES.—The frequencies existing between two definite limits.

BAND-PASS FILTER.—A circuit designed to pass with nearly equal response all currents having frequencies within a definite band and to reduce substantially the amplitudes of currents of all frequencies outside the band.

BASE.—(1) A reference value. (2) A number that is multiplied by itself as many times as indicated by an exponent. (3) Same as radix. (4) Along with emitter and collector, one of the three semiconductor regions of the bipolar type of transistor. (See BIPOLAR TRANSISTOR.)

BASE ADDRESS.—A given address from which an absolute address is derived by combination with a relative address.

BAUD.—A unit of signaling speed equal to the number of discrete conditions or signal events per second. For example, one baud equals one-half dot cycle per second in Morse code, one bit per second in a train of binary signals, and one 3-bit value per second in a train of signals, each of which can assume one of eight different states.

BAUD RATE.—A measure of data flow. The number of signal elements per second based on the duration of the shortest element. When each element carries one bit, the baud rate is numerically equal to bits per second (bps).

used for both mechanical and electrical contact to the chip.

BEAT FREQUENCY.—A frequency resulting from the heterodyning of two different frequencies. It is numerically equal to the difference between or the sum of these two frequencies. (See MIXER.)

BEAT NOTE.—See BEAT FREQUENCY.

BEGINNING-OF-TAPE (BOT) MARKER.—A marker on the magnetic tape, used to indicate the beginning of the permissible recording area; for example, a photo reflective strip or a transparent section of tape.

BIAS.—Vacuum tube—the difference of potential between the control grid and the cathode; transistor—the difference of potential between the base and emitter and the base and collector; magnetic amplifier—the level of flux density in the magnetic amplifier core—under no-signal condition.

BIGFET.—Bipolar Insulated Gate Field-Effect Transistor. A simple integrated circuit combining a field-effect transistor and a bipolar transistor. (See FET.)

BINARY.—(1) Pertaining to a characteristic or property involving a selection, choice, or condition in which there are two possibilities. (2) Pertaining to the number representation system with a radix of two.

BINARY CODE.—A code that makes use of exactly two distinct characters, usually 0 and 1.

BINARY-CODED DECIMAL (BCD) NOTATION.—A system of number representation in which each decimal digit of a number is expressed by binary numbers.

BINARY DIGIT.—In binary notation, either of the digits 0 or 1.

BINARY NOTATION.—Fixed radix notation where the radix is two.

carriers into the base by the emitter and the collection of these minority carriers from the base by the collector. Sometimes called NPN or PNP transistor to emphasize its layered structure. (See BASE, COLLECTOR, and EMITTER.)

BISTABLE.—Pertaining to a device capable of assuming either one of two stable states.

BIT.—A binary digit.

BIT STRING.—A string of binary digits in which the position of each binary digit is considered as an independent unit.

BLANKING.—See GATING.

BLEEDER.—A resistance connected in parallel with a power supply output to protect equipment from excessive voltages if the load is removed or substantially reduced, to improve the voltage regulation, and to drain the charge remaining in the filter capacitors when the unit is turned off.

BLOCK DIAGRAM.—A diagram of a system, instrument, or computer in which the principal parts are represented by suitably associated geometrical figures to show both the basic functions and the functional relationships among the parts. Contrast with FLOWCHART.

BLOCKING CAPACITOR.—A capacitor used to block the flow of direct current while permitting the flow of alternating current.

BOOLEAN.—(1) Pertaining to the processes used in the algebra formulated by George Boole, famous English mathematician and logician. (2) Pertaining to the operations of formal logic.

BOOLEAN ADD.—Same as OR.

BOOLEAN OPERATOR.—A logic operator whose operands and result thereof have one of two values.

BOOTSTRAP.—A technique or device designed to bring itself into a desired state by means of its own action; for example, a machine routine whose first few instructions are sufficient to bring the rest of itself into the computer from an input device.

cuted between two successive decision instructions. (2) Loosely, a conditional jump.

BREAKDOWN VOLTAGE.—The voltage at which an insulator or dielectric ruptures, or at which ionization and conduction take place in a gas or vapor.

BREAKPOINT.—A place in a routine specified by an instruction digit or other condition where the routine may be interrupted by external intervention or by a monitor routine.

BUFFER.—(1) A routine or storage used to compensate for a difference in rate of flow of data or time or occurrence of events when transmitting data from one device to another. (2) An isolating circuit used to prevent a driven circuit from influencing the driving circuit.

BUFFER AMPLIFIER.—An amplifier used to isolate the output of an oscillator from the effects produced by changes in voltage or loading in following circuits.

BUG.—A mistake or malfunction.

BURST.—(1) To separate continuous-form paper into discrete sheets. (2) In data transmission, a sequence of signals counted as one unit in accordance with some specific criterion or measure.

BUS.—One or more conductors used for transmitting signals or power.

BUS BAR.—A primary power distribution point connected to the main power source.

BYPASS CAPACITOR.—A capacitor used to provide an ac path of comparatively low impedance around a circuit element.

BYTE.—A sequence of adjacent binary digits operated upon as a unit and usually shorter than a computer word.

CAPACITANCE.—The property of two or more bodies that enables them to store electrical energy in an electrostatic field between the bodies.

both circuits.

CAPACITIVE REACTANCE (X_c).—The opposition offered to the flow of an alternating current by capacitance, expressed in ohms.

CAPACITOR.—Two electrodes or sets of electrodes in the form of plates, separated from each other by an insulating material called the dielectric.

CAPACITOR STORAGE.—A storage device that uses the capacitance properties of materials to store data.

CARRIAGE CONTROL TAPE.—A tape containing line feed control data for a printing device.

CARRIAGE RETURN.—The operation that prepares for the next character to be printed or displayed at the specified first position on the same line.

CARRIER.—The RF component of a transmitted wave upon which an audio signal or other form of intelligence can be impressed.

CARRY.—(1) One or more digits, produced in connection with an arithmetic operation on a one-digit place of two or more numerals expressed in positional notation and forwarded to another digit place for processing there. (2) The number represented by the digit or digits in (1). (3) Most commonly, a digit, as defined in (1), that arises when the sum or product of two or more digits equals or exceeds the radix of the number representation system.

CATHODE-RAY STORAGE.—An electrostatic storage device that uses a cathode-ray beam for access to the data.

CENTRAL PROCESSING UNIT (CPU).—A unit of a computer that includes the circuits controlling the interpretation and execution of instructions.

CENTRAL PROCESSOR.—A central processing unit.

CHADLESS.—Pertaining to the punching f tape in which chad does not result.

CHAIN PRINTER.—A printer in which the ype slugs are carried by the links of a revolving hain.

CHANNEL.—(1) A path along which signals an be sent; for example, data channel and output channel. (2) The portion of a storage medium that s accessible to a given reading or writing station; for example, track and band.

CHARACTER.—(1) A letter, digit, or other ymbol used as part of the organization, control, or representation of data. A character is often in he form of a spatial arrangement of adjacent or connected strokes.

CHARACTER CHECK.—A check that veri- ies the observance of rules for the formation of characters.

CHARACTER PRINTER.—A device that prints a single character at a time.

CHARACTER RECOGNITION.—The dentification of graphic, phonic, or other haracters by automatic means.

CHARACTER SET.—A set of unique epresentations called characters; for example, he 26 letter of the English alphabet, 0 and 1 of he Boolean alphabet, and the set of signals in he Morse code alphabet.

CHARACTER STRING.—A string con- isting solely of characters.

CHARACTER SUBSET.—A selection of haracters from a character set, comprising all haracters having a specified common feature. For example, in the definition of character set, igits 0 through 9 constitute a character subset.

CHARACTERISTIC IMPEDANCE (Z_o).—The ratio of voltage to current at every point long a transmission line on which there are no tanding waves. (Same as surge impedance.)

CHIP.—Any small piece of semiconductor, especially one fabricated for semiconductor devices.

CHOKE.—A coil that impedes the flow of alternating current of a specified frequency range because of its high inductive reactance at that range.

CHOPPING.—See LIMITING.

CIRCUIT BREAKER.—An electromagnetic or thermal device that opens a circuit when the current in the circuit exceeds a predetermined amount. Circuit breakers can be reset.

CIRCULAR MIL.—An area equal to that of a circle with a diameter of 0.001 inch. It is used for measuring the cross section of wires.

CLAMPING CIRCUIT.—A circuit that maintains either amplitude extreme of a waveform at a certain level of potential.

CLASS A OPERATION.—Operation of a vacuum tube so that plate current flows through the entire operating cycle and distortion is kept to a minimum.

CLASS AB OPERATION.—Operation of a vacuum tube with grid bias so that the operation point is approximately halfway between Class A and Class B.

CLASS B OPERATION.—Operation of a vacuum tube with bias at or near cutoff so that plate current flows during approximately one-half cycle.

CLASS C OPERATION.—Operation of a vacuum tube with bias considerably beyond cutoff so that plate current flows for less than one-half cycle.

CLEAR.—To place one or more storage locations into a prescribed state, usually zero or the space character.

CLIPPING.—See LIMITING.

CLOCK PULSE.—A synchronization signal provided by a clock.

CLOCK TRACK.—A track on which a pattern of signals has been recorded to provide a time reference.

COAXIAL CABLE.—A transmission line consisting of two conductors concentric with and insulated from each other.

COBOL.—(Common Business Oriented Language). A business data processing language.

CODE.—(1) A set of unambiguous rules specifying the way in which data may be represented; for example, the set of correspondences in the standard code for information interchange. (2) In telecommunications, a system of rules and conventions according to which the signals representing data can be formed, transmitted, received, and processed. (3) In data processing, to represent data or a computer program in a symbolic form that can be accepted by a data processor. (4) To write a routine.

COEFFICIENT OF COUPLING (K).—A numerical indication of the degree of coupling existing between two circuits, expressed in terms of either a decimal or a percentage.

COLLECTOR.—Along with the emitter and base, one of the three regions of the bipolar type of transistor. (See BIPOLAR TRANSISTOR.)

COMMUNICATIONS LINK.—The physical means of connecting one location to another for the purpose of transmitting and receiving data.

COMMUTATOR.—The copper segments on the armature of a dc motor or generator. The commutator, which is cylindrical-shaped, is used as a switching device to pass power into or from the brushes of a motor.

generating more than one machine instruction for each symbolic statement, or both, as well as performing the function of an assembler.

COMPILER.—A program that compiles.

COMPUTER.—A data processor that can perform substantial computation, including numerous arithmetic or logic operations, without intervention by an operator.

COMPUTER CODE.—A machine code for a specific computer.

COMPUTER INSTRUCTION.—A machine instruction for a specific computer.

COMPUTER NETWORK.—A complex consisting of two or more interconnected computers.

COMPUTER PROGRAM.—A series of instructions or statements, in a form acceptable to a computer, prepared to achieve a certain result.

COMPUTER WORD.—A sequence of bits or characters treated as a unit and capable of being stored in one computer location. Same as machine word.

CONCURRENT.—Pertaining to the occurrence of two or more events or activities within the same specified interval of time.

CONDENSER.—See CAPACITOR.

CONDITIONAL JUMP.—A jump that occurs if specified criteria are met.

CONDUCTANCE.—The ability of a material to conduct or carry an electric current. It is the reciprocal of the resistance of the material, and is expressed in mhos.

CONDUCTIVITY.—A measure of the ability of a material to act as a path for electron flow. It is the opposite of resistivity and is expressed in mhos per meter.

for communication between the operator or maintenance person and the computer.

CONTROL PANEL.—The part of a computer console containing manual controls.

CONVERT.—To change the representation of data from one form to another; for example, to change numerical data from binary to decimal or from cards to tape.

CONVERTER.—See MIXER.

CORE.—A magnetic material that affords an easy path for magnetic flux lines in a coil.

COULOMB.—A unit of electrical charge; the quantity of electrical charge created by a steady flow of one ampere for one second.

COUNTER.—A device, such as a register or storage location, used to represent the number of occurrences of an event.

COUNTER ELECTROMOTIVE FORCE (EMF).—An EMF induced in a coil or armature that opposes the applied voltage.

COUNTING CIRCUIT.—A circuit that receives uniform pulses representing units to be counted and producing a voltage in proportion to the frequency.

COUPLED IMPEDANCE.—The effect produced in the primary winding of a transformer by the current flowing in the secondary winding.

COUPLING.—The association of two circuits in such a way that energy may be transferred from one to the other.

COUPLING ELEMENT.—The means by which energy is transferred from one circuit to another; the common impedance necessary for coupling.

CRIPPLED MODE.—A system operating with less than full capability, but able to produce a useful product; usually caused by a major component malfunction. Same as degraded mode.

CROSSTALK.—The unwanted energy transferred from one circuit, called the "disturbing" circuit, to another circuit, called the "disturbed" circuit.

CRYSTAL (Xtal).—(1) A natural substance, such as quartz or tourmaline, that is capable of producing a voltage stress when under pressure or producing pressure when under an applied voltage. Under stress, it has the property of responding only to a given frequency when cut to a given thickness. (2) A nonlinear element, such as galena or silicon, in which case the piezoelectric characteristic is not exhibited.

CRYSTAL MIXER.—A device that uses the nonlinear characteristic of a crystal (nonpiezoelectric type) and a point contact to mix two frequencies.

CRYSTAL OSCILLATOR.—An oscillator circuit in which a piezoelectric crystal is used to control the frequency and to reduce frequency instability to a minimum. (See SELF-EXCITED OSCILLATOR.)

CURRENT.—Flow of electrons, measured in amperes.

CURRENT LIMITER.—A protective device similar to a fuse, usually used in high-amperage circuits.

CUTOFF FREQUENCY.—The frequency at which the intrinsic gain of a device falls to some predetermined value. For example, the frequency at which the gain of a bipolar transistor in a common-emitter amplifier configuration is equal to unity.

DARLINGTON PAIR.—A circuit, often integrated, consisting of two bipolar transistors with the collectors connected together and the emitter of one connected to the base of the other. The combination behaves like a very-high-gain transistor. (See SUPERGAIN TRANSISTOR.)

DATA.—(1) A representation of facts, concepts, or instructions in a formalized manner uitable for communication, interpretation, or processing by humans or automatic means. 2) Any representations, such as characters or analog quantities, to which meaning is or might be assigned.

DATA BANK.—A comprehensive collection of libraries of data.

DEBUG.—To detect, locate, and remove mistakes from a routine or malfunctions from a computer. Same as troubleshoot.

DECIBEL (dB).—A term meaning one-tenth of a bel. The ratio of a change in power after attenuation or amplification. An increase in three dB represents double power.

DECIMAL.—Pertaining to the number repreentation system with a radix of 10.

DECIMAL DIGIT.—In decimal notation, one of the characters 0 through 9.

DECIMAL NOTATION.—A fixed radix notation where the radix is 10.

DECIMAL NUMERAL.—A decimal repreentation of a number.

DECIMAL POINT.—The radix point in decimal representation.

DECISION.—A determination of future ction.

DECISION INSTRUCTION.—An instrucion that effects the selection of a branch of a program; for example, a conditional jump nstruction.

DECODE.—To apply a set of unambiguous ules specifying the way in which data may be estored to a previous representation.

DECODER.—(1) A device that decodes. 2) A matrix of logic elements that selects one or more output channels according to the combinaion of input signals present.

DECOUPLING NETWORK.—A network f capacitors, chokes, or resistors, placed in eads that are common to two or more circuits to prevent unwanted interstage coupling.

DEFLECTION SENSITIVITY.—In a CRT, the quotient of the displacement of the electron beam at the place of impact by the change in the deflecting field. It is usually expressed in millimeters per volt applied between the deflection electrodes or in millimeters per gauss of the deflecting magnetic field.

DEGENERATION.—The process whereby a part of the output signal of an amplifying device is returned to its input circuit in such a manner that it tends to cancel part of the input.

DELAY.—The amount of time by which an event is retarded.

DELIMITER.—A flag that separates and organizes items of data. Same as separator.

DEMODULATION.—See DETECTION.

DEMULTIPLEXER.—A hardware device (or software routine) to de-interleave two or more data streams transmitted on a single channel.

DEPLETION LAYER.—The region in a semiconductor where essentially all charge carriers have been swept out by the electric field that existed there.

DESTRUCTIVE READ.—A read process that also erases the data from the source.

DETECTION.—The process of separating the modulation component from the received signal.

DEVELOPMENT TIME.—That part of operating time used for debugging new routines or hardware.

DIAGNOSTIC.—Pertaining to the detection and isolation of a malfunction or mistake.

DIELECTRIC.—An insulator; a term applied to the insulating material between the plates of a capacitor.

DIELECTRIC CONSTANT.—The ratio of the capacitance of a capacitor with a dielectric between the electrodes to the capacitance with air between the electrodes.

DIFFUSION.—Spontaneous intermingling of substances; for example, the diffusion of an impurity into a semiconductor at high temperatures to create a desired concentration of N or P charge carriers.

DIGIT.—A symbol that represents one of the nonnegative integers smaller than the radix. For example, in a decimal notation, a digit is one of the characters from 0 through 9. Same as numeric character.

DIGITAL.—Pertaining to data in the form of digits.

DIGITAL COMPUTER.—(1) A computer in which discrete representation of data is mainly used. (2) A computer that operates on discrete data by performing arithmetic and logic processes on the data.

DIGITIZE.—To use numeric characters to express or represent data.

DIGITIZER.—A software routine or hardware device that converts analog (input) data to digital (output) data.

DIMINISHED RADIX COMPLEMENT.—Same as radix-minus-one complement.

DIODE.—Vacuum tube—a two-element tube that contains a cathode and plate; semiconductor—a material of either germanium or silicon that is manufactured to allow current to flow in only one direction. Diodes are used as rectifiers and detectors.

DIP.—Dual In-line Package. A circuit package somewhat longer than it is wide, with the leads coming out of the two long sides.

DIRECT ACCESS.—(1) Pertaining to the process of obtaining data from or placing data into storage where the time required for such access is independent of the location of the data most recently obtained or placed in storage. (2) Pertaining to a storage device in which the access time is effectively independent of the location of the data. (3) Same as random access.

DISASTER DUMP.—A dump made when a nonrecoverable program error occurs.

DISCRETE.—Pertaining to distinct elements or to representation by means of distinct elements, such as characters.

DISTORTION.—The production of an output waveform that is not a true reproduction of the input waveform. Distortion may consist of irregularities in amplitude, frequency, or phase.

DISTRIBUTED CAPACITANCE.—The capacitance that exists between the turns in a coil or choke, or between adjacent conductors or circuits, as distinguished from the capacitance concentrated in a capacitor.

DISTRIBUTED INDUCTANCE.—The inductance existing along the entire length of a conductor, as distinguished from the self-inductance concentrated in a coil.

DOCUMENTATION.—(1) The creating, collecting, organizing, storing, citing, and disseminating of documents or the information recorded in documents. (2) A collection of documents or information on a given subject.

DONOR.—An impurity that can make a semiconductor N-type by donating extra "free" electrons to the conduction band. The free electrons are carriers of a negative charge.

DOPING.—The introduction of an impurity into the crystal lattice of a semiconductor to modify its electronic properties; for example, adding boron to silicon to make the material more P-type.

DOUBLE PRECISION.—Pertaining to the use of two computer words to represent a number.

DOWNTIME.—The time interval during which a device is malfunctioning.

DRAIN.—Along with the source and gate, one of the three regions of a unipolar or field-effect transistor. (See FET.)

nal, usually because of the effect of noise or tem malfunction.

DROPPING RESISTOR.—A resistor used decrease a given voltage to a lower value.

DRY ELECTROLYTIC CAPACITOR.— electrolytic capacitor using a paste instead a liquid electrolyte. (See ELECTROLYTIC PACITOR.)

DUMP.—(1) To copy the contents of all or t of a storage, usually from an internal rage into an external storage. (2) A process as l). (3) The data resulting from the process as (1).

DYNAMIC DUMP.—A dump performed ing the execution of a computer program.

DYNAMIC STORAGE.—A device which res data in a manner that permits the data to ve or vary with time in such a way that specified data is not always available for overy. Magnetic-drum and disk storage are nvolatile dynamic storage.

DYNAMIC STORAGE ALLOCATION.— storage allocation technique in which the ation of computer programs and data is ermined by criteria applied at the moment of d.

ECCLES-JORDAN CIRCUIT (Trigger cir- t).—A direct-coupled multivibrator circuit ssessing two conditions of stable equilibrium. o known as a flip-flop circuit.

EDDY CURRENT.—Induced circulating rents in a conducting material that are caused a varying magnetic field.

EDIT.—To modify the form or format of a; for example, to insert or delete characters, h as page numbers or decimal points.

EFFECTIVE ADDRESS.—The address that lerived by applying any specified indexing or irect addressing rules to the specified address l that is actually used to identify the current erand.

effective value is also called the RMS value.

EFFICIENCY.—The ratio of output-to-input power, generally expressed as a percentage.

ELECTRIC FIELD.—A space in which an electric charge will experience a force exerted upon it.

ELECTRODE.—A terminal at which electricity passes from one medium into another.

ELECTROLYTE.—A water solution of a substance that is capable of conducting electricity. An electrolyte may be in the form of either a liquid or a paste.

ELECTROLYTIC CAPACITOR.—A capacitor using a metallic plate and an electrolyte as the second plate, separated by a dielectic that is produced by electrochemical action.

ELECTROMAGNET.—A magnet made by passing current through a coil of wire wound on a soft iron core.

ELECTROMAGNETIC FIELD.—A space field in which electric and magnetic vectors at right angles to each other, travel in a direction at right angles to both.

ELECTROMOTIVE FORCE (EMF).—The force that produces an electric current in a circuit.

ELECTRON EMISSION.—The liberation of electrons from a body into space under the influence of heat, light, impact, chemical disintegration, or potential difference.

ELECTRONIC SWITCH.—A circuit that causes a start-and-stop action or a switching action by electronic means.

ELECTRONIC VOLTMETER.—See VACUUM-TUBE VOLTMETER.

ELECTROSTATIC FIELD.—The field of influence between two charged bodies.

EMITTER.—Along with the base and collector, one of the three regions of the bipolar type of transistor. (See BIPOLAR TRANSISTOR.)

ENABLE.—The application of a pulse that prepares a circuit for some subsequent action.

ENCODE.—To apply a set of unambiguous rules specifying the way in which data may be represented in such a manner that a subsequent decoding is possible.

ENCODER.—A device capable of translating from one method of expression to another method of expression; for example, translating a message, "add the contents of A to the contents of B," into a series of binary digits.

END-AROUND CARRY.—A carry from the most significant digit place to the least significant place.

END-OF-FILE (EOF) MARK.—A special character on a magnetic tape used to indicate the end of a set of data.

END-OF-TAPE (EOT) MARK.—A mark on a magnetic tape used to indicate the end of the permissible recording area; for example, a photo reflective strip, a transparent section of tape, or a particular bit pattern.

EQUIVALENT CIRCUIT.—A diagrammatic arrangement of coils, resistors, and capacitors representing the effects of a more complicated circuit to permit easier analysis.

ERROR.—Any discrepancy between a computed, observed, or measured quantity and the true, specified, or theoretically correct value or condition.

ERROR-DETECTING CODE.—A code in which each expression conforms to specific rules of construction, so that, if certain errors occur in an expression, the resulting expression will not conform to the rules of construction and, thus, the presence of the errors is detected. Same as a self-checking code.

the highest and lowest error values.

ERROR RATIO.—The ratio of the number of data units in error to the total number of data units.

EXCLUSIVE OR.—A logic operator having the property that if P is a statement and Q is a statement, then P exclusive OR Q is true if either but not both statements are true, false if both are true or both are false. P exclusive OR Q is often represented by $P \oplus Q$, $P \veebar Q$. Contrast with OR.

EXECUTIVE ROUTINE.—A routine that controls the execution of other routines.

EXPONENT.—In a floating point representation, the numeral, or a pair of numerals representing a number, that indicates the power to which the base is raised.

FARAD (f).—The unit of capacitance.

FAULT.—A physical condition that causes a device, a component, or an element to fail to perform in a required manner; for example, a short circuit, a broken wire, or an intermittent connection.

FEEDBACK.—A transfer of energy from the output circuit of a device back to its input.

FEEDBACK LOOP.—The components and processes involved in correcting or controlling a system by using part of the output as input.

FERRITE.—An iron compound frequently used in the construction of magnetic cores.

FET.—Field-Effect Transistor. A transistor consisting of a source, gate, and drain, whose action depends on the flow of majority carriers past the gate from source to drain. The flow is controlled by the transverse electric field under the gate. (See UNIPOLAR TRANSISTOR, BIGFET, DRAIN, and IGFET.)

FIC.—Film Integrated Circuit. See THIN-FILM INTEGRATED CIRCUIT.

ata, for example, a group of card columns used o represent a wage rate or a set of bit locations n a computer word used to express the address f the operand.

FIELD INTENSITY.—Electrical or magnetic trength of a field.

FIELD WINDING.—The coil used to provide ne magnetizing force in motors and generators.

FILM INTEGRATED CIRCUIT (FIC).—ee THIN-FILM INTEGRATED CIRCUIT.

FILTER.—(1) A device or program that eparates data, signals, or material in accordance ith specified criteria. (2) A mask. (3) A ombination of circuit elements designed to pass definite range of frequencies, attenuating all thers.

FIRST DETECTOR.—See MIXER.

FIXED BIAS.—A bias voltage of constant alue, such as one obtained from a battery, ower supply, or generator.

FIXED CAPACITOR.—A capacitor that as no provision for varying its capacitance.

FIXED-CYCLE OPERATION.—An opera- on that is completed in a specified number of egularly timed execution cycles.

FIXED RESISTOR.—A resistor that has no rovision for varying its resistance.

FIXED STORAGE.—Storage whose contents re not alterable by computer instructions; for xample, magnetic core storage with a lockout eature or photographic disk. Examples of fixed torage include nonerasable storage, permanent torage, and read-only storage.

FLAG.—(1) Any of various types of indi- ators used for identification; for example, a ordmark. (2) A character that signals the ccurrence of some condition, such as the nd of a word. (3) Same as mark, sentinel, and ag.

Eccles-Jordan circuit and toggle.

FLOATING-POINT REPRESENTATION.—A number representation system in which each number, as represented by a pair of numerals, equals one of those numerals times a power of an implicit-fixed positive integer base where the power is equal to the implicit base raised to the exponent represented by the other numeral.

Common Notation

0.0001234 or $(0.1234) \times (10^{-3})$

A Floating Representation

1234 – 03

FLOWCHART.—A graphical representation for the definition, analysis, or solution of a problem in which symbols are used to represent operations, data, flow, equipment, and so forth.

FLOWCHART SYMBOL.—A symbol used on a flowchart to represent data, flow, equipment or an operation.

FLOWCHART TEXT.—The descriptive information associated with flowchart symbols.

FLOW DIRECTION.—In flowcharting, the antecedent-to-successor relation, indicated by arrows or other conventions, between operations on a flowchart.

FLOWLINE.—On a flowchart, a line representing a connecting path between flowchart symbols.

FLORESCENCE.—The property of emitting light as the immediate result of electronic bombardment.

FLUX FIELD.—All electric or magnetic lines of force in a given region.

FLY-BACK.—The portion of the time base during which the spot is returning to the starting point. This is usually not seen on the screen of the cathode-ray tube because of gating action or the rapidity with which it occurs.

FORMAT.—The arrangement of data.

FORTRAN.—(FORmula TRANslating system). A language primarily used to express computer programs by arithmetic formulas.

FRAME.—An area, one recording position long, extending across the width of a magnetic or paper tape perpendicular to its movement. Several bits or punch positions may be included in a single frame through the use of different recording positions across the width of the tape.

FREE ELECTRONS.—Electrons that are loosely held and, consequently, tend to move at random among the atoms of the material.

FREE OSCILLATIONS.—Oscillatory currents that continue to flow in a tuned circuit after the impressed voltage has been removed. Their frequency is the resonant frequency of the tuned circuit.

FREQUENCY.—The number of complete cycles per second existing in any form of wave motion, such as the number of cycles per second of an alternating current.

FREQUENCY DISTORTION.—Distortion that occurs as a result of failure to amplify or attentuate equally all frequencies present in a complex wave.

FREQUENCY MODULATION.—See MODULATION.

FREQUENCY STABILITY.—The ability of an oscillator to maintain its operation at a constant frequency.

FULL-WAVE RECTIFIER CIRCUIT.—A circuit that uses both the positive and the negative alternations of an alternating current to produce a direct current.

FUNCTIONAL DIAGRAM.—A diagram that represents the functional relationships among the parts of a system.

FUSE.—A protective device inserted in series with a circuit. It contains a metal that will melt or break when current is increased beyond a specific value for a definite period of time.

GAIN (A).—The ratio of the output power, voltage, or current to the input power, voltage, or current, respectively.

GALVANOMETER.—An instrument used to measure small dc currents.

GATE.—(1) Along with the source and drain, one of the three regions of the unipolar or field-effect transistor. (See FET.) (2) A device having one output channel and one or more input channels, such as the output channel state is completely determined by the input channel states, except during switching transients; for example, AND GATE, OR GATE.

GATING (Cathode-ray tube).—Application of a rectangular voltage to the grid or cathode of a cathode-ray tube to sensitize it during the sweep time only.

GENERAL-PURPOSE COMPUTER.—A computer that is designed to handle a wide variety of problems, as contrasted with a special-purpose computer.

GENERATOR.—A machine that converts mechanical energy into electrical energy.

GRAY CODE.—A binary code in which sequential numbers are represented by binary expressions, each of which differs from the preceding expression in one place only. Same as a reflected binary code.

GROUND.—A metallic connection with the earth to establish ground potential. Also, a common return to a point of zero RF potential, such as the chassis of a receiver or of a transmitter.

HALF-ADDER.—A combinational logic element having two outputs, S and C, and two inputs, A and B, in such a manner that the outputs are related to the inputs according to the following table:

INPUT		OUTPUT	
A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

S denotes "Sum Without Carry"; C denotes "Carry." Two half-adders may be used for performing binary addition.

passed and the other half is blocked by the action of the rectifier, thus producing pulsating direct current.

HALF-WORD.—A contiguous sequence of bits or characters that comprises half a computer word and is capable of being addressed as a unit.

HARDWARE.—Physical equipment, as opposed to the computer program or method of use; for example, mechanical, magnetic, electrical, or electronic devices. Contrast with software.

HARMONIC.—An integral multiple of a fundamental frequency. (The second harmonic s twice the frequency of the fundamental or first harmonic.)

HARMONIC DISTORTION.—See AMPLITUDE DISTORTION.

HEAD.—A device that reads, writes, or erases data on a storage medium; for example, a small electromagnet used to read, write, or erase data on a magnetic drum or tape, or the set of perforating, reading, or making devices used for punching, reading, or printing on paper tape.

HENRY (h).—The basic unit of inductance.

HELMHOLTZ COIL.—A variometer having horizontal and vertical balanced coil windings, used to vary the angle of phase difference between any two similar waveforms of the same frequency.

HERTZ (Hz).—A unit of frequency. Formerly called cycle per second.

HETERODYNE.—To beat or mix two signals of different frequencies.

HEXADECIMAL.—Same as sexadecimal.

HIC.—Hybrid Integrated Circuit. Consists of an assembly of one or more semiconductor devices and a thin-film integrated circuit on a single substrate, usually of ceramic.

HIGH-SPEED CARRY.—Any technique in parallel addition for speeding up carry propagation.

HOLE.—The absence of a valence electron in a semiconductor crystal. The motion of a hole is equivalent to the motion of a positive charge.

HOLE PATTERN.—A punching configuration within a card column that represents a single character of a character set.

HOLLERITH.—Pertaining to a particular type of code or punched card, which uses 12 rows per column and usually 80 columns per card.

HYBRID COMPUTER.—A computer for data processing using both analog representation and discrete representation of data.

HYSTERESIS.—A lagging of the magnetic flux in a magnetic material behind the magnetizing force that is producing it.

IDENTIFIER.—A symbol whose purpose is to identify, indicate, or name a body of data.

IDLE TIME.—That part of available time during which the hardware is not being used.

IGFET.—A field-effect transistor whose gate is insulated from the semiconductor by a thin intervening layer of insulator, usually thermal oxide.

ILLEGAL CHARACTER.—A character or combination of bits that is not valid according to some criteria; for example, a character that is not a member of a specified alphabet.

IMPATT DIODE.—Impact Avalanche and Transit Time diode. An avalanche diode used as a high-frequency oscillator or amplifier. Its negative resistance depends upon the transit time of charge carriers through the depletion layer. (See AVALANCHE MULTIPLICATION.)

offered to the flow of an alternating current. It may consist of any combination of resistance, inductive reactance, and capacitive reactance.

IMPEDANCE COIL.—See CHOKE.

IMPEDANCE COUPLING.—The use of a tuned circuit or an impedance coil as the common coupling element between two circuits.

IMPULSE.—Any force acting over a comparatively short period of time, such as a momentary rise in voltage.

INCONNECTOR.—In flowcharting, a connector that indicates a continuation of broken flowline.

INDEX.—(1) An ordered reference list of the contents of a file or document together with keys of reference notations for identification or location of those contents. (2) To prepare a list as in (1). (3) A symbol of a numeral used to identify a particular quantity in an array of similar quantities. For example, the terms of an array of similar quantities or the terms of an array represented by X 1/2, X2, . . ., X100 have the indexes 1, 2, (4). (See INDEX REGISTER.)

INDEX REGISTER.—A register whose contents may be added to or subtracted from the operand address prior to or during the execution of a computer instruction.

INDEXED ADDRESS.—An address modified by the content of an index register prior to or during the execution of a computer instruction.

INDIRECT ADDRESS.—An address that specifies a storage location containing either a direct address or another indirect address. Contrast with direct address.

INDUCTANCE (L).—The property of a circuit that tends to oppose a change in the existing current.

INDUCTION.—The act or process of producing voltage by the relative motion of a magnetic field across a conductor.

opposition to the flow of alternating or pulsating current caused by the inductance of a circuit. It is measured in ohms.

INDUCTOR.—A circuit element designed so that its inductance is its most important electrical property; a coil.

INFINITE.—Extending indefinitely; having innumerable parts, capable of endless division within itself.

INHERITED ERROR.—An error carried forward from a previous step in a sequential process.

INHIBITING SIGNAL.—A signal that prevents an operation from taking place.

INITIAL PROGRAM LOADER (IPL).—The procedure that causes the initial part of an operating system or other program to be loaded in such a manner that the program can then proceed under its own control. Contrast with bootstrap.

INITIALIZE.—To set counters, switches, and addresses to zero or other starting values at the beginning of, or at prescribed points in, a computer routine. Same as prestore.

INJECTION.—In a semiconductor, the introduction of excess minority carriers. Injection can take place at a conducting PN junction or in a region illuminated by light.

IN PHASE.—Applied to the condition that exists when two waves of the same frequency pass through their maximum and minimum values of like polarity at the same instant.

INPUT.—(1) Pertaining to a device, process, or channel involved in the insertion of data or states or to the data or states involved. (2) One or a sequence of input states.

INPUT AREA.—An area of storage reserved for input. Same as input block.

INPUT CHANNEL.—A channel for impressing a state on a device or logic element.

INPUT DATA.—Data to be processed.

INPUT/OUTPUT (I/O).—Pertaining to either input, output, or to both.

INSTALLATION TIME.—Time spent in installing and testing either hardware, software, or both.

INSTANTANEOUS VALUE.—The magnitude at any particular instant when a value is continually varying with respect to time.

INSTRUCTION.—A statement that specifies an operation and the values or locations of its operands.

INSTRUCTION ADDRESS.—The address that must be used to fetch an instruction.

INSTRUCTION COUNTER.—A counter that indicates the location of the next computer instruction to be interpreted.

INSTRUCTION REGISTER.—A register that stores an instruction for execution.

INSTRUCTION REPERTOIRE.—The set of operations that can be represented in a given operation code.

INTEGRATED CIRCUIT.—A circuit in which many elements are fabricated and interconnected by a single process, as opposed to a nonintegrated circuit in which the transistors, diodes, resistors, and so on, are fabricated separately and then assembled.

INTEGRATED DATA PROCESSING (IDP).—Data processing in which the coordination of data acquisition and all other stages of data processing is achieved in a coherent system; for example, a business data processing system in which data for orders and buying is combined to accomplish the functions of scheduling, invoicing, and accounting.

INTEGRATING CIRCUIT.—A circuit that produces an output voltage substantially in proportion to the frequency and amplitude of the input voltage.

of the brilliance of the trace on the screen of a cathode-ray tube in conformity with the signal.

INTERFACE.—A shared boundary. An interface might be a hardware component to link two devices, or it might be a portion of storage or registers accessed by two or more computer programs.

INTERFACE STATES.—Extra donors, acceptors, or traps that may occur at a boundary between a semiconductor and some other material.

INTERLEAVE.—To arrange parts of one sequence of things or events so that they alternate with parts of one or more other sequences of things or events so that each sequence retains its identity; for example, to organize storage into banks with independent bases so that sequential data references may be overlapped in a given period of time.

INTERNAL STORAGE.—Addressable storage directly controlled by the central processing unit of a digital computer.

INTERPRETER.—(1) A computer program that translates and executes each source language statement before translating and executing the next one. (2) A device that prints on a punched card the data already punched in the card.

INTER-RECORD GAP.—An area on a data medium used to indicate the end of a block or record.

INTERRUPT.—To stop a process in such a way that it can be resumed.

INTRINSIC CONDUCTIVITY.—Electrical conductivity of an apparently pure material—that is, without the presence of any significant impurities.

INVERSE PEAK VOLTAGE.—The highest instantaneous negative potential that the plate can acquire with respect to the cathode without danger of damaging the tube.

INVERT.—To change a physical or logical state to its opposite.

ION.—An elementary particle of matter or a small group of such particles having a net positive or negative charge.

IONIZATION.—Process by which ions are produced in solids, liquids, and gases.

IONIZATION POTENTIAL.—The lowest potential at which ionization takes place within a gas-filled tube.

JFET.—Junction Field-Effect Transistor (see FET) in which the gate electrode is formed by a PN junction.

JOULE.—A unit of energy or work. A joule of energy is liberated by one ampere flowing for one second through a resistance of one ohm.

JUMP.—A departure from the normal sequence of executing instructions in a computer. Same as transfer.

JUNCTION.—The interface between two semiconductor regions of differing conductivity. Usually refers to a PN junction, at which the conductivity changes from P-type to N-type.

JUNCTION TRANSISTOR.—A bipolar transistor constructed from interacting PN junctions. The term is used to distinguish junction transistors from other types, such as field-effect and point-contact transistors. (See BIPOLAR TRANSISTOR and PN JUNCTION.)

JUSTIFY.—(1) To adjust the printing positions of characters on a page so that the lines have the desired length and that both the left- and right-hand margins are regular. (2) By extension, to shift the contents of a register so that the most or the least significant digit is at some specified position in the register.

KEYPUNCH.—A keyboard-actuated device that punches holes in a card to represent data.

KILO (k).—A prefix meaning 1000.

KILOHERTZ (kHz).—1000 hertz.

computer program.

LAG.—(1) The delay between two events. (2) The amount one wave is behind another wave in time; expressed in electrical degrees.

LAMINATED CORE.—A core built up from thin sheets of metal and used in transformers and relays.

LANGUAGE.—A set of representations, conventions, and rules used to convey information.

LASER.—Light Amplification by Stimulated Emission of Radiation. In the laser, excited electrons give up their excitation in step with the light that is passing by to add energy to the transmitted light. Some lasers can generate or amplify extremely pure colors, in very narrow beams, often with very high intensity.

LEAD.—The opposite of lag. Also, a wire or connection.

LEADER.—The blank section of tape at the beginning of a reel of tape.

LEAKAGE.—Electrical loss caused by poor insulation.

LED.—Light-Emitting Diode. A semiconductor device in which the energy of minority carriers in combining with holes is converted to light. Usually, but not necessarily, constructed as a PN junction device.

LEFT-JUSTIFY.—(1) To adjust the printing positions of characters on a page so that the left margin of the page is regular. (2) By extension, to shift the contents of a register so that the most significant digit is at some specified position of the register.

LEVEL.—The degree of subordination in a hierarchy.

LIFETIME.—Term used to describe the life of a minority charge carrier in a semiconductor crystal; for example, how long a free electron exists in a P-type material before it combines with a hole and is neutralized.

LIMITING.—Removal by electronic means f one or both extremities of a waveform at a redetermined level.

LINEAR.—Having an output that varies in irect proportion to the input.

LINE-BALANCE CONVERTER.—A device sed at the end of a coaxial line to isolate the uter conductor from ground.

LINE OF FORCE.—A line in an electric or agnetic field that shows the direction of the orce.

LINE PRINTER.—A device that prints all haracters of a line as a unit.

LINE PRINTING.—The printing of an ntire line of characters as a unit.

LINKAGE.—In programming, coding that onnects two separately coded routines.

LOAD.—(1) The impedance to which energy being supplied. (2) The power that is being elivered by any power-producing device. The quipment that uses the power from the power- roducing device. (3) In programming, to enter ata into storage or working registers.

LOCAL OSCILLATOR.—The oscillator sed in a superheterodyne receiver, the output f which is mixed with the desired RF carrier to orm the intermediate frequency.

LOCATION.—Any place in which data may e stored.

LOGICAL FILE.—A collection of one or ore logical records.

LOGIC ELEMENT.—A device that per- orms a logic function.

LOGIC INSTRUCTION.—An instruction at executes an operation defined in symbolic gic, such as AND, OR, NOR.

LOGIC SHIFT.—A shift that affects all ositions.

LOGIC SYMBOL.—(1) A symbol used to present a logic element graphically. (2) A mbol used to represent a logic operator.

LOOP.—A sequence of instructions executed repeatedly until a terminal condition prevails.

LOOSE COUPLING.—Less than critical coupling; coupling providing little transfer of energy.

LSI.—Large-Scale Integration. (At the beginning of the LSI era, a count of 100 gates qualified for LSI. Today, an 8-bit CPU can be fabricated on a single chip.)

MACHINE CODE.—An operation code that a machine is designed to recognize.

MACHINE INSTRUCTION.—An instruction that a machine can recognize and execute.

MACHINE LANGUAGE.—A language used directly by a machine.

MACHINE WORD.—Same as computer word.

MACROCOMMAND.—A program entity formed by a string of standard, but related, commands that are put into effect by a single macrocommand. Any group of frequently used commands can be combined into a macrocommand.

MACROINSTRUCTION.—An instruction in a source language equivalent to a specified sequence of machine instructions.

MACROPROGRAMMING.—Programming with macroinstructions.

MAGNETIC AMPLIFIER.—A saturable reactor type of device used in a circuit to amplify or control.

MAGNETIC CARD.—A card with a magnetic surface on which data can be stored by selective magnetization of portions of the flat surface.

MAGNETIC CIRCUIT.—The complete path of magnetic lines of force.

essential to its use. It may be used to concentrate an induced magnetic field as in a transformer nduction coil, or armature, to retain a magnetic polarization for storing data or for its nonlinear properties as in a logic element. It may be made of such material as iron, iron oxide, or ferrite and in such shapes as wires, tapes, toroids, rods, or thin film.

MAGNETIC DELAY LINE.—A delay line whose operation is based on the time of propagation of magnetic waves.

MAGNETIC DISK.—A flat circular plate with a magnetic surface on which data can be stored by selective magnetization of portions of the flat surface.

MAGNETIC DRUM.—A right-rotating circular cylinder with a magnetic surface on which data can be stored by selective magnetization of portions of the curved surface.

MAGNETIC FIELD.—The space in which a magnetic force exists.

MAGNETIC FLUX.—The total number of lines of force issuing from a pole of a magnet.

MAGNETIC HYSTERESIS LOOP.—A closed curve showing the relation between the magnetization force and the induction of magnetization in a magnetic substance when the magnetized field (force) is carried through a complete cycle.

MAGNETIC INK.—An ink that contains particles of a magnetic substance whose presence can be detected by magnetic sensors.

MAGNETIC STORAGE.—A storage device that uses the magnetic properties of materials to store data; for example, magnetic cores, tapes, and films.

MAGNETIC TAPE.—(1) A tape with a magnetic surface on which data can be stored by selective polarization of portions of the surface. (2) A tape of magnetic material used as the constituent in some forms of magnetic cores.

MAGNETIZE.—To convert a material into a magnet by causing the molecules to rearrange.

MAGNETO.—A generator that produces alternating current and has a permanent magnet as its field.

MAGNETOSTRICTION.—A change in the physical size of a magnetic material produced by the effect of a magnetic field.

MAIN FRAME.—Same as central processing unit.

MAIN STORAGE.—The general-purpose storage of a computer. Usually, main storage can be accessed directly by the operating registers.

MAINTENANCE.—Any activity intended to eliminate faults or to keep hardware or programs in satisfactory working condition, including tests, measurements, replacements, adjustments, and repairs.

MAINTENANCE TIME.—Time used for preventive and corrective maintenance of hardware.

MAJORITY CARRIER.—The mobile charge carrier (hole or electron) that predominates in a semiconductor material; for example, electrons in an N-type region.

MANTISSA.—The fractional part of a logarithm.

MARGINAL CHECK.—A preventive maintenance procedure in which certain operating conditions, such as supply voltage or frequency, are varied about their nominal values to locate defects before they become serious.

MARK.—Same as flag.

MASK.—(1) Pattern, or template, used in photolithographic-like processes used in making integrated circuits. The pattern prescribes regions of the circuit electrical leads, and so forth. (2) A pattern of characters used to control the retention or elimination of portions of another pattern of characters. (3) A filter.

MASS STORAGE DEVICE.—A device aving a large storage capacity; for example, a nagnetic disk or magnetic drum.

MASTER FILE.—A file that is either relaively permanent or that is treated as an authority n a particular job.

MATCH.—To check for identity between wo or more items of data.

MATCHED IMPEDANCE.—The condition hat exists when two coupled circuits are adjusted o that their impedances are equal.

MATHEMATICAL MODEL.—A mathenatical representation of a process, device, or oncept.

MATRIX.—(1) In mathematics, a two-dimenional rectangular array of quantities. Matrices re manipulated in accordance with the rules of natrix algebra. (2) In computers, a logic network n the form of an array of input leads and output eads with logic elements connected at some of heir intersections. (3) By extension, an array of ny number of dimensions.

MATRIX STORAGE.—Storage, the elenents of which are arranged in such a manner hat access to any location requires the use of wo or more coordinates; for example, cathodeay storage and magnetic core storage.

MEDIUM.—The material, or configuration hereof, on which data is recorded; for example, aper tape, cards, and magnetic tape. Synonynous with data medium.

MEGA (M).—A prefix meaning one million.

MEGAHERTZ (MHz).—One million hertz.

MEGGER.—A test instrument used to neasure insulation resistance and other high esistances. It is a portable hand-driven dc enerator used as an ohmmeter.

MEGOHM (abbreviated MEG).—A million hms.

MERGE.—To combine items from two or nore similarly ordered sets into one set that is rranged in the same order.

MHO.—The unit of conductance.

MICRO (μ).—A prefix meaning one millionth.

MICROINSTRUCTION MEMORY.—The part of a computer system into which information can be inserted and held for future use. Storage and memory are interchangeable expressions. Memories accept and hold binary numbers only. Memory types are core, disk, drum, and semiconductor.

MICROPROCESSOR.—A central processing unit fabricated on one or more chips. While there is no standard design in existing units, a number of well-delineated areas are present in all of them: arithmetic & logic unit, control block, and register array. When joined to a memory storage system, the resulting combination is referred to in today's usage as a *microcomputer*. Each microprocessor is supplied with an instruction set, and this software manual may be just as important to the user as the hardware.

MICROSECOND (μs).—One millionth of a second.

MILLI (m).—A prefix meaning one thousandth.

MILLIAMPERE (mA).—One thousandth of an ampere.

MINORITY CARRIER.—The nonpredominant mobile charge carrier in a semiconductor; for example, electrons in a P-type region.

MIXER.—A vacuum tube or crystal and suitable circuit used to combine the incoming and local-oscillator frequencies to produce an intermediate frequency. (See BEAT FREQUENCY.)

MNEMONIC SYMBOL.—A symbol chosen to assist the human memory; for example, an abbreviation such as "mpy" for "multiply."

MODEM.—(MOdulator-DEModulator). A device that modulates or demodulates signals transmitted over communication facilities.

ance with other signals in order to convey intelligence. The modulating signal may be an audiofrequency signal, video signal (as in television), or electrical pulses or tones to operate relays, and so forth.

MODULATOR.—The circuit that provides the signal, which varies the amplitude, frequency, or phase of the resultant wave in a transmitter.

MODULE.—(1) A program unit that is discrete and identifiable with respect to compiling, combining with other units, and loading; for example, the input to, or output from, an assembler, compiler, linkage editor, or executive routine. (2) A packaged functional hardware unit designed for use with other components.

MODULUS.—The number of permissible numbers used in a process or system. For example, if only the integers from −15 to +15 inclusive are considered, 31 is the modulus of this set of numbers.

MONITOR.—Software or hardware that observes, supervises, controls, or verifies the operations of a system.

MONOLITH.—A semiconductor chip containing a multiplicity of devices interconnected into an integrated circuit.

MONOSTABLE.—Pertaining to a device that has one stable state.

MOS.—Metal Oxide Semiconductor. The structure of an MOS Field Effect Transistor (FET) is metal over silicon oxide over silicon. The metal electrode is the gate; the silicon oxide is the insulator; and carrier-doped regions in the silicon substrate become the drain and source. The result is a sandwich very much like a capacitor, which explains why MOS is slower than bipolar since the "capacitor sandwich" must charge up before current can flow.

MOSFET.—A field-effect transistor containing a metal gate over thermal oxide over silicon. The MOSFET structure is one way to make an IGFET.

MULTIPLE PUNCHING.—The punching of more than one hole in the same column of a punched card by means of more than one keystroke.

MULTIPLEX.—To interleave or simultaneously transmit two or more messages on a single channel.

MULTIPROCESSING.—Pertaining to the simultaneous execution of two or more computer programs or sequences of instructions by a computer or computer network.

MULTIPROCESSOR.—A computer employing two or more processing units under integrated control.

MULTIPROGRAMMING.—Pertaining to the concurrent execution of two or more programs by a computer.

MULTIVIBRATOR.—A type of relaxation oscillator for the generation of nonsinusoidal waves in which the output of each of its two tubes or transistors is coupled to the input of the other to sustain oscillations.

MUTUAL INDUCTANCE.—A circuit property existing when the relative position of two inductors causes the magnetic lines of force from one to link with the turns of the other.

NAND.—A logic operator having the property that if P is a statement, Q is a statement, R is a statement,...then the NAND OF P, Q, R,...is true if at least one statement is false, false if all statements are true. Same as NOT-AND.

N-CORE-PER-BIT STORAGE.—A storage device that uses n magnetic cores for each bit to be stored.

NDR.—See NONDESTRUCTIVE READ.

NEGATE.—To perform the logic operation NOT.

NEGATIVE CHARGE.—The electrical charge carried by a body that has an excess of electrons.

NEON BULB.—A glass bulb containing two ctrodes in neon gas at low pressure.

NETWORK.—Any electrical circuit conning two or more interconnected elements.

NIXIE.—An electronic tube type device that plays letters, alphabetic symbols, or numerals the means of a common annode and 10 ferent cathodes.

NODE.—A zero point; specifically, a rent node is a point of zero current and a age node is a point of zero voltage.

NOISE.—(1) Random variations of one more characteristics of any entity, such as age, current, or data. (2) A random signal known statistical properties of amplitude, ribution, and spectral density. (3) Loosely, disturbance tending to interfere with the mal operation of a device or system.

NONDESTRUCTIVE READ (NDR).—A d process that does not erase the data in the rce.

NONINDUCTIVE CAPACITOR.—A capac- in which the inductive effects at high frencies are reduced to a minimum.

NONINDUCTIVE CIRCUIT.—A circuit in ch inductance is reduced to a minimum or ligible value.

NONLINEAR.—Having an output that s not vary in direct proportion to the input.

NONRETURN-TO-ZERO (MARK) Z(M)) RECORDING.—A method of record- in which ones are represented by a change he condition of magnetization; zeros are esented by the absence of change.

NONRETURN-TO-ZERO (NRZ) RECORD- G.—A method of recording in which the nge between the state of magnetization esenting either zero or one provides the rence condition. Same as nonreturn-to-refere recording.

NOR.—A logic operator having the property that if P is a statement, Q is a statement, R is a statement,...then the NOR of P, Q, R,...is true if all statements are false, false if at least one statement is true. P NOR Q is often represented by a combination of "OR" and "NOT" symbols, such as ∼(PVQ). P NOR Q is also called "neither P nor Q." Same as NOT-OR.

NORMAL DIRECTION FLOW.—A flow in a direction from left to right or from top to bottom on a flowchart.

NORMALIZE.—(1) To multiply a variable or one or more quantities occurring in a calculation by a numerical coefficient to make an associated quantity assume a nominated value; for example, to make a definite integral of a variable, or the maximum member of a set of quantities, equal to unity. (2) Loosely, a scale.

NOT.—A logic operator having the property that if P is a statement, then the NOT of P is true if P is false, false if P is true. The NOT of P is often represented by $\bar{P}$, $\sim P$, $\urcorner P$, P'.

NOT-AND.—Same as NAND.

NOT-OR.—Same as NOR.

NPN.—A semiconductor structure consisting of a layer of P-type material sandwiched between layers of N-type material, as commonly used in the bipolar type of transistor.

N-TYPE.—Semiconductor material in which the majority carriers are electrons and are therefore negative.

NUCLEUS.—The core of an atom. It is comprised mainly of protons and neutrons and is the part of the atom that has the most mass.

NULL.—Zero.

NUMBER.—(1) A mathematical entity that may indicate quantity or amount of units. (2) Loosely, a numeral.

NUMBER REPRESENTATION SYSTEM.—An agreed set of symbols and rules for number representation.

NUMBER SYSTEM.—Loosely, a number representation system.

NUMERAL.—(1) A discrete representation of a number. For example, twelve, 12, XII, and 1100 are four different numerals that represent the same number. (2) A numeric word that represents a number.

NUMERIC WORD.—A word consisting of digits and possibly space characters and special characters.

OBJECT CODE.—Output from a compiler or assembler that is itself an executable machine code or is suitable for processing to produce an executable machine code.

OBJECT PROGRAM.—A fully compiled or assembled program ready for loading into the computer. Same as target program.

OCTAL.—(1) Pertaining to a characteristic or property involving a selection, choice, or condition in which there are eight possibilities. (2) Pertaining to the number representation system with a radix of eight.

OCTET.—A byte composed of eight bits.

ODD-EVEN CHECK.—Same as parity check.

OFF LINE.—Pertaining to equipment or devices not under control of the central processing unit.

OFF-LINE STORAGE.—Storage not under control of the central processing unit.

OHM(Ω).—The unit of electrical resistance.

OHMIC CONTACT.—Contact to a semiconductor or other part of a device having low electrical resistance and not showing rectifying behavior. (See RECTIFYING CONTACT.)

one complement in binary notation.

ON LINE.—(1) Pertaining to equipment or devices under control of the central processing unit. (2) Pertaining to a user's ability to interact with a computer.

ON-LINE STORAGE.—Storage under control of the central processing unit.

OPEN CIRCUIT.—A circuit that does not provide a complete path for the flow of current.

OPENENDED.—Pertaining to a process or system that can be augmented.

OPERAND.—That which is operated upon. An operand is usually identified by an address part of an instruction.

OPERATING SYSTEM.—Software that controls the execution of computer programs and which may provide scheduling, debugging, input/output control, accounting, compilation, storage assignment, data management, and related services.

OPERATING TIME.—That part of available time during which the hardware is operating and assumed to be yielding correct results. It includes development time, production time, and makeup time.

OPERATION.—A program step undertaken or executed by a computer; for example, addition, multiplication, extraction, comparison, shift, and transfer. The operation is usually specified by the operator part of an instruction.

OPERATION CODE.—A code that represents specific operations. Same as instruction code.

OPERATION DECODER.—A device that selects one or more control channels according to the operator part of a machine instruction.

OPERATOR.—(1) In the description of a process, that which indicates the action to be performed on operands. (2) A person who operates a machine.

es.

PTICAL SCANNER.—(1) A device that optically and usually generates an analog ital signal. (2) A device that optically scans d or written data and generates digital sentations thereof.

PTIMUM COUPLING.—See CRITICAL PLING.

R.—A logic operator having the property f P is a statement, Q is a statement, R is a nent,. . . , then OR of P, Q, R,. . . is true if ast one statement is true, false if all nents are false. P OR Q is often represented + Q, P V Q. Same as inclusive OR, boolean logical add. Contrast with exclusive OR.

R GATE.—A gate that implements the "OR" operator.

SCILLATOR.—A circuit capable of con- g direct current into alternating current of quency determined by the constant of the t.

SCILLATORY CIRCUIT.—A circuit in oscillations can be generated or sustained.

SCILLOGRAPH.—See OSCILLOSCOPE.

SCILLOSCOPE.—An instrument for ng graphical representations of the wave- encountered in electrical circuits.

UTCONNECTOR.—In flowcharting, a ctor that indicates a point at which a ne is broken for continuation at another

UTPUT.—Pertaining to a device, process, annel involved in an output process or to ata or states involved.

UTPUT AREA.—An area of storage ed for output.

UTPUT CHANNEL.—A channel for ying data from a device or logic element.

OUTPUT DEVICE.—The device or collective set of devices used for conveying data from another device.

OUTPUT PROCESS.—The process of delivering data by a system, subsystem, or device.

OUTPUT STATE.—The state occurring on a specified output channel.

OVERDRIVEN AMPLIFIER.—An amplifier designed to distort the input signal waveform by a combination of cut-off limiting and saturation limiting.

OVERFLOW.—That portion of the result of an operation that exceeds the capacity of the intended unit of storage.

OVERLOAD.—A load greater than the rated load of an electrical device.

OXIDE MASKING.—Use of an oxide on a semiconductor to create a pattern in which impurities are diffused or implanted.

OXIM.—Oxide-Isolated Monolith. A method of making integrated circuits in which an oxide layer is introduced to insulate semiconductor regions from each other.

PACK.—To compress data in a storage medium by taking advantage of known characteristics of the data in such a way that the original data can be recovered; for example, to compress data in a storage medium by making use of bit or byte locations that would otherwise go unused.

PACKING DENSITY.—The number of useful storage cells per unit of dimension; for example, the number of bits per inch stored on a magnetic tape or drum track.

PARALLEL.—Pertaining to the simultaneous occurrence of two or more related activities in multiple devices or channels.

PARALLEL FEED.—Application of a dc voltage to the plate or grid of a tube in parallel with an ac circuit so that the dc and ac components flow in separate paths. Also called shunt feed.

capacitor and an inductor. (Same as tank circuit.)

PARAMETER.—A variable that is given a constant value for a specific purpose or process.

PARAPHASE AMPLIFIER.—An amplifier that converts a single input into a push-pull output.

PARITY BIT.—A check bit appended to an array of binary digits to make the sum of all the binary digits, including the check bit, always odd or always even.

PARITY CHECK.—A check that tests whether the number of ones (or zeros) in an array of binary digits is odd or even.

PARTIAL CARRY.—In parallel addition, a technique in which some or all of the carries are stored temporarily instead of being allowed to propagate immediately.

PASS.—One cycle of processing a body of data.

PASSIVATION.—Treatment of a region of a device to prevent deterioration of electronic properties through chemical action or corrosion. Usually, passivation protects against moisture and other contaminants. (See SEALED JUNCTION.)

PATCH.—To modify a routine in a rough or expedient way.

PATTERN RECOGNITION.—The identification of shapes, forms, or configurations by automatic means.

PATTERN-SENSITIVE FAULT.—A fault that appears in response to some particular pattern of data.

PEAKING CIRCUIT.—A type of circuit that converts an input to a peaked output waveform.

PEAK VALUE.—The maximum instantaneous value of a varying current, voltage, or power. It is equal to 1.414 times the effective value of a sine wave.

provide the system with outside communication.

PERMALLOY.—An alloy of nickel and iron having an abnormally high magnetic permeability. (See PERMEABILITY.)

PERMEABILITY.—A measure of the ease with which magnetic lines of force can flow through a material as compared to air.

PHASE DIFFERENCE.—The time in electrical degrees by which one wave leads or lags another.

PHASE INVERSION.—A phase difference of 180° between two similar waveships of the same frequency.

PHASE-SPLITTING CIRCUIT.—A circuit which produces, from the same input waveform, two output waveforms that differ in phase from each other.

PHOSPHORESCENCE.—The property of emitting light for some time after excitation by electronic bombardment.

PHOTODIODE.—An optically sensitive diode. Often the current is accurately proportional to the intensity of the incident light.

PHOTOLITHOGRAPHIC PROCESS.—A technique used in making integrated circuits, which uses light and selective masking to develop a fine-scaled pattern of areas in a semiconductor; analogous to processes using photo negatives in offset printing.

PHOTORESIST.—A photosensitive material which, after selective exposure to ultraviolet light, resists the action of a chemical. Used in conjunction with a mask to selectively process certain areas of a semiconductor device.

PIEZOELECTRIC EFFECT.—The effect of producing a voltage by placing a stress, either by compression, expansion, or twisting, on a crystal and, conversely, the effect of producing a stress in a crystal by applying a voltage to it.

PINBOARD.—A perforated board into which pins are manually inserted to control the operation of equipment.

PIPELINE COMPUTERS.—Computers that execute only serial programs.

PLA.—Programmed Logic Array. An orderly arrangement of logical AND logical OR functions. Its application is similar to that of a glorified ROM. The PLA is primarily a combinational logic device.

PLANAR STRUCTURE.—A flat-surfaced device structure fabricated by diffusion and oxide masking, with the junctions terminating on a single plane. The structural planarity is often advantageous for photoresist processing.

PLUGBOARD.—A perforated board into which plugs are manually inserted to control the operation of equipment.

PN JUNCTION.—Within a crystal, an interface between a P region that conducts primarily by holes and an N region that conducts primarily by electrons.

PNIP.—Semiconductor crystal structure consisting of layers that are successively P-type, N-type, intrinsic, and P-type. Used for high-voltage, high-frequency bipolar transistors.

PNP.—Semiconductor crystal structure consisting of an N-type region sandwiched between two P-type regions; commonly used in bipolar transistors.

PNPN.—A semiconductor crystal structure in which the layers are successively P-type, N-type, P-type, and N-type. When ohmic contacts are made to the various layers, a silicon controlled rectifier (SCR), or thyristor, results.

POINT-CONTACT TRANSISTOR.—The original transistor, invented at Bell Laboratories, which was made by placing sharp metal points in contact with the surface of an N-type semiconductor crystal.

POLARITY.—The character of having magnetic poles or electric charges.

POLLING.—The method used to identify the source of interrupt requests. When several interrupts occur at one time, the control program decides which one to service first.

POLYPHASE.—A circuit that uses more than one phase of alternating current.

POSITIONAL NOTATION.—A numeration system in which a number is represented by means of an ordered set of digits in such a way that the value contributed by each digit depends upon its position and upon its value.

POSITIVE CHARGE.—The electrical charge carried by a body that has become deficient in electrons.

POSITIVE FEEDBACK.—See REGENERATION.

POTENTIAL.—The amount of charge held by a body as compared to another point or body, usually measured in volts.

POTENTIOMETER.—A variable voltage divider; a resistor having a variable contact arm, so that any portion of the potential applied between its ends may be selected.

POWER.—The rate of doing work or the rate of expanding energy. The unit of electrical power is the watt.

POWER AMPLIFICATION.—The process of amplifying a signal to produce a gain in power, as distinguished from voltage amplification. The gain in the ratio of the alternating power output to the alternating power input of an amplifier.

POWER FACTOR.—The ratio of the actual power of an alternating or pulsating current, as measured by a wattmeter, to the apparent power, as indicated by ammeter and voltmeter readings. The power factor of an inductor, capacitor, or insulator is an expression of the losses.

PREDEFINED PROCESS.—A process identified only by name and defined elsewhere.

PREVENTIVE MAINTENANCE.—Maintenance specifically intended to prevent faults from occurring during subsequent operation. Contrast with corrective maintenance. Corrective maintenance and preventive maintenance are both performed during maintenance time.

PREVENTIVE MAINTENANCE TIME.—Time, usually scheduled, used to perform preventive maintenance.

PRIMARY CIRCUIT.—The first, in electrical order, of two or more coupled circuits, in which a change in current induces a voltage in the other or secondary circuits, such as the primary winding of a transformer.

PRIME MOVER.—The source of mechanical power used to drive the rotor of a generator.

PROBLEM DESCRIPTION.—(1) In information processing, a statement of a problem. The statement may also include a description of the method of solution, the procedures, algorithms, and so forth.

PROBLEM-ORIENTED LANGUAGE.—A programming language designed for the convenient expression of a given class of problems.

PROCESS.—A systematic sequence of operations to produce a specified result.

PROCESSOR.—(1) In hardware, a data processor. (2) In software, a computer program that includes the compiling, assembling, translating, and related functions for a specific programming language.

PROGRAM.—(1) A series of actions proposed to achieve a certain result. (2) Loosely, a routine. (3) To design, write, and test a program as in (1). (4) Loosely, to write a routine.

PROGRAM COUNTER.—One of the registers in the central processing unit that holds addresses necessary to step the machine through the program. During the interrupts, the program counter saves the address of the instruction. Branching also requires loading of the return address in the program counter.

that appears in response to some particular sequence of program steps.

PROGRAMMING FLOWCHART.—A flowchart representing the sequence of operations in a program.

P-TYPE.—Semiconductor material in which the majority carriers are holes and are therefore positive.

PULSATING CURRENT.—A unidirectional current that increases and decreases in magnitude.

PULSE-REPETITION RATE.—The number of pulses per unit time.

PUNCH.—A perforation, as in a punched card or paper tape.

PUNCHED TAPE.—A tape on which a pattern of holes or cuts is used to represent data.

PUSH-PULL CIRCUIT.—A push-pull circuit usually refers to an amplifier circuit using two vacuum tubes or solid-state devices in such a fashion that when one device is operating on a positive alternation, the other device is operating on a negative alternation.

Q.—(1) The symbol used to denote a quantity of electrical charge. (2) The figure of merit of efficiency of a circuit or coil. Numerically, it is equal to the inductive reactance divided by the resistance of the circuit or coil.

QUANTIZE.—To subdivide the range of values of a variable into a finite number of nonoverlapping, but not necessarily equal, subranges or intervals, each of which is represented by an assigned value within the subrange.

QUASI-INTRINSIC.—Descriptive of a semiconductor material whose conductivity is kept low, close to the intrinsic value, by doping with impurities, which create carrier traps lying near the center of the energy gap.

RADIAL TRANSFER.—An input process or an output process.

RADIATE.—To emit energy, such as RF waves, into space.

RADIATION RESISTANCE.—A fictitious resistance that would dissipate the same power that the antenna dissipates.

RADIX.—In positional representation, that integer, if it exists, by which the significance of the digit place must be multiplied to give the significance of the next higher digit place.

RADIX COMPLEMENT.—A complement obtained by subtracting each digit from one less than its radix, then adding one to the least significant digit, executing all carries required.

RADIX-MINUS-ONE COMPLEMENT.—A complement obtained by subtracting each digit from one less than the radix.

RADIX NOTATION.—A positional representation in which the significance of any two adjacent digit positions has an integral ratio called the radix of the less significant of the two positions; permissible values of the digit in any position range from zero to one less than the radix of that position.

RADIX POINT.—In radix notation, the real or implied character that separates the digits associated with the integral part of a numeral from those associated with the fractional part.

RALU.—Register, Arithmetic, and Logic Unit. Unlike the discrete ALU package that functions as an arithmetic and logic unit only, the ALU in the RALU is equipped with a number of registers.

RAM.—Random Access Memory. Random in the sense of providing access to any storage location point in the memory immediately by means of vertical and horizontal coordinates. Information may be "written" in or "read" out in the same rapid way.

RANDOM ACCESS.—An access mode in which specific logical records are obtained from or placed into a mass storage file in a nonsequential manner.

RANDOM NUMBERS.—A series of numbers obtained by chance.

RATE, BIT.—The rate at which binary digits, or pulses representing them, pass a given point on a communications line or channel.

RATE, CLOCK.—The time rate at which pulses are emitted from the clock. The clock rate determines the rate at which logical or arithmetic gating is performed with a synchronous computer.

RATIO.—The value obtained by dividing one number by another, indicating their relative proportions.

REACTANCE (X).—The opposition offered to the flow of an alternating current by the inductance, capacitance, or both, in any circuit.

READ.—To acquire or interpret data from a storage device, a data medium, or any other source.

READ-IN.—To sense information contained in some source and transmit this information to an internal storage.

READOUT.—To sense information contained in some internal storage and transmit this information to a storage external to the computer.

REAL TIME.—Pertaining to the actual time during which a physical process transpires.

REAL-TIME INPUT.—Input data inserted into a system at the time of generation by another system.

REAL-TIME OUTPUT.—Output data removed from a system at time of need by another system.

RECIPROCAL.—The value obtained by dividing the number 1 by any quantity.

RECOMBINATION.—In a semiconductor, the combining of holes and electrons. Recombination tends to reduce the minority carriers to their equilibrium number after injection has taken place. (See LIFETIME.)

RECORD.—A collection of related items of data, treated as a unit; for example, one line of an invoice may form a record, and a complete set of such records may form a file.

RECORDING DENSITY.—The number of bits in single linear track measured per unit of length of the recording medium.

RECORD LAYOUT.—The arrangement and structure of data in a record, including the sequence and size of its components. By extension, a record layout might be the description thereof.

RECORD LENGTH.—A measure of the size of a record, usually specified in units, such as words or characters.

RECTIFIERS.—Devices used to change alternating current to unidirectional current. These may be vacuum tubes, semiconductors such as germanium and silicon, dry-disk rectifiers such as selenium and copper-oxide, and also certain types of crystal.

RECTIFYING CONTACT.—An electrical contact through which current flows easily in one direction (the "forward" direction), but with difficulty or not at all in the reverse direction.

REFLECTED IMPEDANCE.—See COUPLED IMPEDANCE.

REGENERATION.—The process of returning a part of the output signal of an amplifier to its input circuit in such a manner that it increases the total amplification. Same as positive feedback or regenerative feedback.

REGISTER.—A device capable of storing a specified amount of data, such as one word.

REGISTRATION.—The accurate positioning relative to a reference.

REGULATION (voltage).—The ratio of the change in voltage because of a load to the open-circuit voltage, expressed as a percentage.

RELATIVE ADDRESS.—The number that specifies the difference between the absolute address and the base address.

RELAXATION OSCILLATOR.—A circuit for the generation of nonsinusoidal waves by gradually storing and quickly releasing energy either in the electric field of a capacitor or in the magnetic field of an inductor.

RELAY.—An electromechanical switching device that can be used as a remote control.

RELIABILITY.—The probability that a device will perform without failure for a specified time period or amount of usage.

RELOCATE.—In computer programming, to move a routine from one portion of storage to another and to adjust the necessary address references so that the routine, in its new location, can be executed.

RELUCTANCE.—A measure of the opposition that a material offers to magnetic lines of force.

REMOTE ACCESS.—Pertaining to communication with a data processing facility by one or more stations that are distant from that facility.

REMOTE STATION.—Data terminal equipment for communicating with a data processing system from a location that is time, space, or electrically distant.

REPERFORATOR.—REceiving PERFORATOR.

REPETITION INSTRUCTION.—An instruction that causes one or more instructions to be executed an indicated number of times.

RESET.—(1) To restore a storage device to a prescribed initial state, not necessarily that denoting zero. (2) To place a binary cell into the state denoting zero.

RESISTANCE (R).—The opposition to the flow of current caused by the nature and physical dimensions of a conductor.

RESISTOR.—A circuit element whose chief characteristic is resistance; used to oppose the flow of current.

RESONANCE CURVE.—A graphical repre- entation of the manner in which a resonant ircuit responds to various frequencies at and ear the resonant frequency.

RESTART.—To reestablish the execution of a outine, using the data recorded at a checkpoint.

RETENTIVITY.—The measure of the ability f a material to hold its magnetism.

RHEOSTAT.—A variable resistor.

RIGHT-JUSTIFY.—(1) To adjust the print- ig positions of characters on a page so that the ght margin of the page is regular. (2) To shift ie contents of a register so that the least signifi- ant digit is at some specified position of the egister.

RIPPLE VOLTAGE.—The fluctuations in ie output voltage of a rectifier, filter, or enerator.

RISE TIME.—For an instantaneous change ı voltage applied, the time required for the teady-state current to rise from 10 percent to 90 ercent of its maximum value.

RMS.—Abbreviation for root-mean-square. See EFFECTIVE VALUE.)

ROM.—Read Only Memory. In its virgin tate, the ROM consists of a mosaic of undiffer- ntiated cells. One type of ROM is programmed y mask pattern as part of the last manufacturing tage. Another, more popular type better known s PROM, is programmable in the field with he aid of programmer equipment. Program ata stored in ROMs is often called firmware ecause the data cannot be altered. However, nother type of PROM is now on the market alled EPROM, which is erasable by ultraviolet rradiation and is electrically reprogrammable.

ROUNDING ERROR.—An error resulting rom roundoff.

ROUND OFF.—To delete the least signifi- ant digit, or digits, of a numeral and to adjust he part retained in accordance with some rule.

sequence of operations. (2) A subdivision of a program consisting of two or more instructions that are functionally related; therefore, a program.

ROW.—A horizontal arrangement of characters or other expressions.

ROW BINARY.—Pertaining to the binary representation of data on cards in which the significances of punch positions are assigned along the card rows. For example, each row in an 80-column card may be used to represent 80 consecutive binary digits.

RUN.—A single, continuous performance of a computer program or routine.

SATURABLE REACTOR.—A control device that uses a small dc current to control a large ac current by controlling core flux density.

SATURATION.—The condition existing in any circuit when an increase in the driving signal produces no further change in the resultant effect.

SATURATION POINT.—The point beyond which an increase in either grid voltage, plate voltage, or both, produces no increase in the existing plate current.

SCALE.—To adjust the representation of a quantity by a factor to bring its range within prescribed limits.

SCALE FACTOR.—A number used as a multiplier, so chosen that it will cause a set of quantities to fall within a given range of values.

SCAN.—To examine sequentially, part by part.

SCHEDULED MAINTENANCE.—Maintenance carried out in accordance with an established plan.

SCHOTTKY BARRIER.—A potential barrier formed between a metal and a semiconductor. The term usually refers to a barrier that is high enough and thick enough to serve as a rectifier, but avoids the slowing-down effects that result from injection of charge in PN junction rectifiers.

(See PNPN and THYRISTOR.)

SCRATCHPAD.—Information that the processing unit stores or holds temporarily. It is a memory containing subtotals for various unknowns needed for final results.

SEALED JUNCTION.—A PN junction sealed by covering it with an inert material that does not allow troublesome impurities to reach the junction and cause changes in its electrical characteristics. (See PASSIVATION.)

SEARCH.—To examine a set of items for one or more having a desired property.

SECONDARY.—The output coil of a transformer. (See PRIMARY CIRCUIT.)

SEGMENT.—(1) To divide a computer program into parts in such a way that the program can be executed without the entire program being in internal storage at any one time. (2) A part of a computer program as in (1).

SELECTION CHECK.—A check that verifies the choice of devices, such as registers, in the execution of an instruction.

SELECTIVITY.—The degree to which a receiver is capable of discriminating between signals of different carrier frequencies.

SELF-EXCITED OSCILLATOR.—An oscillator depending on its resonant circuits for frequency determination. (See CRYSTAL OSCILLATOR.)

SELF-INDUCTION.—The production of a counterelectromotive force in a conductor when its own magnetic field collapses or expands with a change in current in the conductor.

SEMICONDUCTOR.—An element, such as silicon or germanium, with resistivity in the range between metals and insulators, in which the electric-charge-carrier concentration increases with increasing temperature over some temperature range.

SEQUENCE.—An arrangement of items according to a specified set of rules.

SEQUENTIAL.—Pertaining to the occurrence of events in time sequence, with little or no simultaneous occurrence or overlap of events.

SEQUENTIAL CONTROL.—Defined sequence until a different sequence is explicitly initiated by a jump instruction.

SEQUENTIAL LOGIC.—A circuit arrangement in which the output state is determined by the previous state of the input.

SEQUENTIAL LOGIC ELEMENT.—A device having at least one output channel and one or more input channels, all characterized by discrete states in such a way that the state of each output channel is determined by the previous states of the input channels.

SEQUENTIAL OPERATION.—Pertaining to the performance of operations one after the other.

SERIAL.—(1) Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.

SERIES FEED.—Application of a dc voltage to the plate or grid of a tube through the same impedance in which the alternating current flows. Compare with Parallel Feed.

SERIES RESONANCE.—The condition existing in a circuit when the source of voltage is in series with an inductor and capacitor whose reactances cancel each other at the applied frequency and thus reduce the impedance to minimum.

SERIES-RESONANT CIRCUIT.—A resonant circuit in which the capacitor and the inductor are in series with the applied voltage.

SERIES-WOUND.—A motor or generator in which the armature is wired in series with the field winding.

SERVO.—A device used to convert a small movement into one of greater movement or force.

SERVOMECHANISM.—A closed-loop system that produces a force to position an object in accordance with the information that originates at the input.

SET.—(1) A collection. (2) To place a storage device into a specified state, usually other than that denoting zero or space character. (3) To place a binary cell into the state denoting one.

SETUP.—(1) In a computer consisting of an assembly of individual computing units, the arrangement of interconnections between the units and the adjustments needed for the computer to solve a particular problem. (2) An arrangement of data or devices to solve a particular problem.

SETUP DIAGRAM.—A diagram specifying a given computer setup.

SEXADECIMAL.—(1) Pertaining to a characteristic or property involving a selection, choice, or condition in which there are 16 possibilities. (2) Pertaining to the numeration system with a radix of 16. Same as hexadecimal.

SHIELDING.—A metallic covering used to prevent magnetic or electrostatic coupling between adjacent circuits.

SHIFT.—A movement of data to the right or left.

SHIFT REGISTER.—A register in which the stored data can be moved to the right or left.

SHORT CIRCUIT.—A low-impedance or zero impedance path between two points.

SHUNT.—Parallel. A parallel resistor placed in an ammeter to increase its range.

SHUNT FEED.—See PARALLEL FEED.

interconnected.

SIGN BIT.—A binary digit occupying the sign position.

SIGN DIGIT.—A digit occupying the sign position.

SIGN POSITION.—A position, normally located at one end of a numeral, that contains an indication of the algebraic sign of the number.

SIGNIFICANCE.—In positional representation, the factor by which a digit is multiplied to obtain its additive contribution in the representation of a number; the factor is determined by the digit position.

SIGNIFICANT DIGIT.—A digit needed for a certain purpose, particularly one that must be kept to preserve a specific accuracy or precision.

SILICON CONTROLLED RECTIFIER.—See SCR.

SINE WAVE.—The curve traced by the projection on a uniform time scale off the end of a rotating arm, or vector. Also known as a sinusoidal wave.

SINGLE-CRYSTAL MATERIAL.—A material all of which consists of a single crystal, as distinct from most materials, which are polycrystalline or multiple crystal.

SKEW.—The angular displacement of a symbol or data medium from the intended or ideal placement.

SKIN EFFECT.—The tendency of alternating currents to flow near the surface of a conductor. Thus, they are restricted to a small part of the total cross-sectional area, which increases the resistance and becomes more marked as the frequency rises.

SKIP.—To ignore one or more instructions in a sequence of instructions.

SNAP-OFF DIODE.—A kind of diode which, when switched from a forward to a reverse direction, passes current for a short time and then very rapidly turns off. The sudden change in current is very rich in harmonics. Used as a frequency multiplier or pulse generator.

SOFTWARE.—A set of computer programs, procedures, and possibly associated documentation concerned with the operation of a data processing system; for example, compilers, library routines, manuals, and circuit diagrams.

SOLAR CELL.—Large-area diode in which a PN junction near the surface of a semiconductor converts solar energy into electrical energy.

SOLENOID.—A multiturn coil of wire wound in a uniform layer or layers on a hollow, cylindrical form.

SOLID-STATE COMPONENT.—A component whose operation depends on the control of electric or magnetic phenomena in solids; for example, a transistor, crystal diode, or a ferrite core.

SOLID-STATE ELECTRONICS.—Designation used to describe devices and circuits fabricated from solid materials, such as semiconductors, ferrites, or films, as distinct from devices and circuits using electron tube technology.

SORT.—To segregate items in groups according to some definite rules. Same as order.

SORTER.—A person, device, or computer routine that sorts.

SOURCE.—Along with the gate and drain, one of the three regions of the unipolar or field-effect transistor. (See FET.)

SOURCE LANGUAGE.—The language from which a statement is translated.

SOURCE PROGRAM.—A computer program written in a source language.

the space between the cathode and plate in a vacuum tube because the cathode emits more electrons than are immediately attracted to the plate.

SPECIAL CHARACTER.—A graphic character that is neither a letter, a digit, nor a space character.

SPECIAL-PURPOSE COMPUTER.—A computer designed to handle a restricted class of problems, as contrasted with a general-purpose computer.

SPOT PUNCH.—A device for punching one hole at a time.

SPREADING RESISTANCE.—The ohmic resistance of a small ohmic contact to a large volume of semiconductor material.

STABILITY.—Freedom from undesired variation.

STATIC.—A fixed, nonvarying condition; without motion.

STATIC CHARACTERISTICS.—The characteristics of a tube with no output load and with dc potentials applied to the grid and plate.

STATIC DUMP.—A dump performed at a particular point in time with respect to a machine at the end of a run.

STORAGE.—(1) Pertaining to a device into which data can be entered, in which it can be held, and from which it can be retrieved at a later time. (2) Loosely, any device that can store data.

STORAGE ALLOCATION.—The assignment of blocks of data to specified blocks of storage.

STORAGE CAPACITY.—The amount of data that can be contained in a storage device.

STORAGE CELL.—An elementary unit of storage.

STORAGE PROTECTION.—An arrangement for preventing access to storage for either reading, or writing, or both.

STORAGE TIME.—The time required to withdraw the minority carriers from both sides of a PN junction when the junction is switched from a forward to a reverse bias.

STORE.—(1) To transfer an element of information to a device from which the unaltered information can be obtained at a later time. (2) To retain data in a device from which it can be obtained at a later time.

STORED-PROGRAM COMPUTER.—A computer controlled by internally stored instructions that can synthesize, store, and, in some cases, alter instructions as though they were data and that can subsequently execute these instructions.

SUBROUTINE.—A routine that can be part of another routine.

SUBROUTINE CALL.—The subroutine, in object coding, that performs the call function.

SUBSTRATE.—The underlying material upon which a device, circuit, or epitaxial layer is fabricated.

SUPERGAIN TRANSISTOR.—A transistor with a common emitter current gain of about a thousand or more, usually fabricated as a Darlington pair.

SUPERHETERODYNE.—A receiver in which the incoming signal is mixed with a locally generated signal to produce a predetermined intermediate frequency.

SURFACE STATES.—Extra donors, acceptors or traps, usually undesired, which may occur on a semiconductor surface because of crystal imperfections or contamination and which may vary undesirably with time.

SURGE.—Sudden changes of current or voltage in a circuit.

SWEEP CIRCUIT.—The part of a cathode-ray oscilloscope that provides a time-reference base.

SWING.—The variation in frequency or amplitude of an electrical quantity.

SWINGING CHOKE.—A choke with an effective inductance that varies with the amount of current passing through it. Used in some power-supply filter circuits.

SWITCH.—A device or programming technique for making a selection; for example, a toggle or a conditional jump.

SYMBOL.—A representation of something by reason of relationship, association, or convention.

SYMBOL STRING.—A string consisting solely of symbols.

SYMBOLIC ADDRESS.—An address expressed in symbols convenient to the computer programmer.

SYMBOLIC CODING.—Coding that uses machine instructions with symbolic addresses.

SYMBOLIC LOGIC.—The discipline that treats formal logic by means of a formalized artificial language or symbolic calculus whose purpose is to avoid the ambiguities and logical inadequacies of natural languages.

SYNCHRONIZATION PULSES.—Pulses introduced by transmitting equipment into the receiving equipment to keep the two equipments operating in step.

SYNCHRO SYSTEM.—An electrical system that gives remote indications or control by means of self-synchronizing motors.

SYNCHRONOUS.—Happening at the same time; having the same period and phase.

SYNTAX.—(1) The structure of expressions in a language. (2) The rules governing the structure of a language.

TABLE.—A collection of data in which each tem is uniquely identified by a label, by its osition relative to the other items, or by some ther means.

TABLE LOOKUP.—A procedure for ob- aining the function value corresponding to an rgument from a table of function values.

TACHOMETER.—An instrument for meas- ring revolutions per minute.

TANK CIRCUIT.—See PARALLEL-RESO- NANT CIRCUIT.

TAPE DRIVE.—A device that moves tape ast a head.

TAPE TO CARD.—Pertaining to equip- nent or methods that transmit data from either nagnetic tape or punched tape to punched ards.

TAPE TRANSPORT.—Same as tape drive.

TAPE UNIT.—A device containing a tape rive, together with reading and writing heads nd associated controls.

TEMPORARY STORAGE.—In pro- ramming, storage locations reserved for inter- nediate results. Same as working storage.

TERMINAL.—A point in a system or com- nunications network at which data can either nter or leave.

TERTIARY WINDING.—A third winding n a transformer or magnetic amplifier that is sed as a second control winding.

THERMAL OXIDE.—On silicon semicon- luctor devices, an oxide fabricated by exposing he silicon to oxygen at high temperatures. The esulting interface is completely free of ionic mpurities and defects.

THERMISTOR.—A resistor used to com- ensate for temperature variations in a circuit.

THERMOCOUPLE AMMETER.—An ammeter that operates by means of a voltage produced by the heating effect of a current passed through the junction of two dissimilar metals. It is used for RF measurements.

THIN FILM.—Loosely, magnetic thin film.

THIN-FILM INTEGRATED CIRCUIT.—A circuit consisting of patterns of tantalum or other materials laid down on a substrate of glass or ceramic, typically larger than silicon integrated circuits. Sometimes called FIC.

THYRISTOR.—A PNPN device useful as a controlled rectifier that can conduct high currents by injection of a highly conducting hole-electron plasma. So called by analogy to a thyratron electron tube. Same as SCR.

TIGHT COUPLING.—Degree of coupling in which practically all the magnetic lines of force produced by one coil link a second coil.

TIME SHARE.—To use a device for two or more interleaved purposes.

TOGGLE.—(1) Same as flip-flop. (2) Pertaining to any device having two stable states.

TRACE.—A visible line or lines appearing on the screen of a cathode-ray tube in operation.

TRACING ROUTINE.—A routine that provides a historical record of specified events in the execution of a program.

TRACK.—The portion of a moving storage medium, such as a drum, tape, or disk, that is accessible to a given reading head position.

TRANSFORM.—To change the form of data according to specific rules.

TRANSFORMER.—A device composed of two or more coils, linked by magnetic lines of force, used to transfer energy from one circuit to another.

TRANSISTOR.—A semiconductor device that uses a stream of charge carriers to produce active electronic effects. The name was coined from the electrical characteristic of "transfer resistance." As compared with electron tubes, transistors are usually advantageous because of their greater efficiency, lifetime, reliability, and compactness.

TRANSIT TIME.—(1) The time a charge carrier takes to go from one part of a semiconductor to another. For example, in a reverse-biased diode, the time a carrier requires to move through the depletion region. (2) The time electrons take to travel between the cathode and the plate of a vacuum tube.

TRANSLATE.—To transform statements from one language to another without significantly changing the meaning.

TRANSMISSION.—The sending of data from one location and the receiving of data in another location, usually leaving the source data unchanged.

TRANSMISSION LINES.—Any conductor or system of conductors used to carry electrical energy from its source to a load.

TRANSMIT.—To send data from one location and to receive the data at another location.

TRAPS.—Impurities or defects in a semiconductor that can capture an electron or hole and hold it for a period of time. After trapping, the carriers may be released or recombined, with probability depending on trap energy. Recombination of minority carriers is expedited by the presence of "deep" traps, so the lifetime of a minority carrier can be varied by varying the type and concentration of trap impurities.

TRIGGERING.—Starting an action in another circuit, which then functions for a time under its own control.

TROUBLESHOOT.—Same as debug.

TRUNCATION ERROR.—An error resulting from truncation.

TRUTH TABLE.—A table that describes a logic function by listing all possible combinations of input values and indicating, for each combination, the true output values.

TUNED CIRCUIT.—A resonant circuit.

TUNNEL DIODE.—A diode that exhibits negative resistance because of tunneling through a thin depletion layer.

TUNNELING.—In quantum mechanics, a process that explains how charge carriers can penetrate insulating regions that are sufficiently thin.

TWELVE PUNCH.—A punch in the top row of a Hollerith punch card. Same as y-punch.

TWO-OUT-OF-FIVE CODE.—A positional notation in which each decimal digit is represented by five binary digits of which two are one kind (for example, ones), and three are the other kind (for example, zeros).

TWOS COMPLEMENT.—The radix complement in binary notation.

TYPE FONT.—Type of a given size and style; for example, 10-point Bodoni Modern.

UNBALANCED LINE.—A transmission line in which the voltages on the two conductors are not equal with respect to ground; for example, a coaxial line.

UNIDIRECTIONAL.—Flowing in only one direction; for example, direct current.

UNIPOLAR TRANSISTOR.—A transistor, such as a FET, whose action depends on majority charge carriers only.

UNIT.—(1) A device having a special function. (2) A basic element.

special registers for the storage of operands, and results supplemented by shifting and sequencing circuitry for implementing multiplication, division, and other desired operations.

UNIT CONTROL.—The portion of a computer that directs the sequence of operations, interprets the coded instructions, and initiates the proper commands to the computer circuits preparatory to execution.

UNPACK.—To recover the original data from packed data.

UTILITY ROUTINE.—Same as service routine.

VACUUM-TUBE VOLTMETER (VTVM).—A device that uses either the amplifier characteristic or the rectifier characteristic of a vacuum tube, or both, to measure either dc or ac voltages. Its input impedance is very high, and the current used to actuate the meter movement is not taken from the circuit being measured. The VTVM can be used to obtain accurate measurements in sensitive circuits.

VARACTOR DIODE.—A diode making use of the variation of capacitance that takes place as reverse bias is varied. Can be used as a frequency multiplier, as a tuning element in a tuned circuit, or as a low-noise parametric amplifier.

VARIABLE.—A quantity that can assume any of a given set of values.

VARIABLE-LENGTH RECORD.—Pertaining to a file in which the records are not uniform in length.

VARIABLE-POINT REPRESENTATION.—A positional representation in which the position of the radix point is explicitly indicated by a special character at that position.

VARIOCOUPLER.—Two independent inductors, so arranged mechanically that their mutual inductance (coupling) can be varied.

VECTOR.—A line used to represent both direction and magnitude.

VELOCITY MODULATION.—A method of modulation in which the input signal voltage is used to change the velocity of electrons in a constant current electron beam so that the electrons are grouped into bunches.

VENN DIAGRAM.—A diagram in which sets are represented by closed regions.

VERIFY.—(1) To determine whether a transcription of data or other operation has been accomplished accurately. (2) To check the results of keypunching.

VIDEO AMPLIFIER.—A circuit capable of amplifying a very wide range of frequencies, including and exceeding the audio band of frequencies.

VOLATILE STORAGE.—A storage device in which stored data is lost when the applied power is removed; for example, an acoustic delay line.

VOLT (V).—The unit of electrical potential.

VOLTAGE AMPLIFICATION.—The process of amplifying a signal to produce a gain in voltage. The voltage gain of an amplifier is the ratio of its alternating-voltage output to its alternating-voltage input.

VOLTAGE DIVIDER.—An impedance connected across a voltage source. The load is connected across a fraction of this impedance so that the load voltage is substantially in proportion to this fraction.

VOLTAGE DOUBLER.—A method of increasing the voltage by rectifying both halves of a cycle and causing the outputs of both halves to be additive.

VOLTAGE REGULATION.—A measure of the degree to which a power source maintains its output-voltage stability under varying load conditions.

WATT (W).—The unit of electrical power.

WATTMETER.—An instrument for meas- ring electric power in watts.

WAVE.—Generally, an electromagnetic im- ılse, periodically changing in intensity and aveling through space. More specifically, the aphical representation of the intensity of that npulse over a period of time.

WAVEFORM.—The shape of the wave ob- ined when instantaneous values of an ac uantity are plotted against time in rectangular ordinates.

WAVELENGTH (λ).—The distance, usually pressed in meters, traveled by a wave during e time interval of one complete cycle. It is ual to the velocity divided by the frequency.

WEIGHT.—Same as significance.

WIEN-BRIDGE CIRCUIT.—A circuit in ich the various values of capacitance and sistance are made to balance with each other at certain frequency.

WORD.—(1) A character string or a bit ing considered as an entity. (2) See computer ord, half-word, machine word, and numeric ord.

WRITE.—To record data in a storage device or data medium. The recording need not be permanent, such as the writing on a cathode-ray tube display device.

X.—The symbol for reactance.

Y-PUNCH.—Same as twelve punch.

Z.—The symbol for impedance.

ZENER DIODE.—A voltage-limiting diode with high impedance at low voltages, but low impedance above a "breakdown" voltage. Most voltage-limiting diodes break down by impact ionization ("avalanche") rather than by cold-field emission (the Zener effect).

ZEROFILL.—To character fill with the representation of zero.

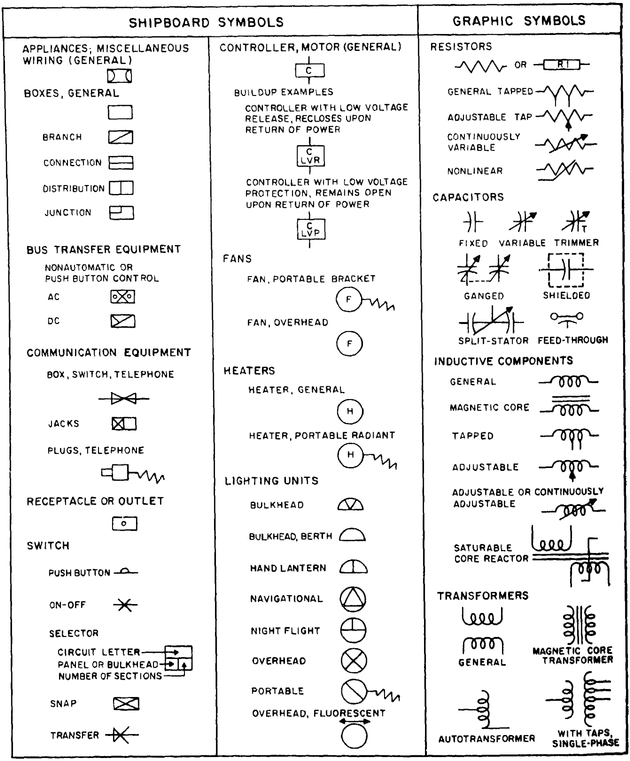
ZERO SUPPRESSION.—The elimination of nonsignificant zeros in a numeral.

ZONE PUNCH.—A punch in the eleven, twelve, or zero row of a punched card.

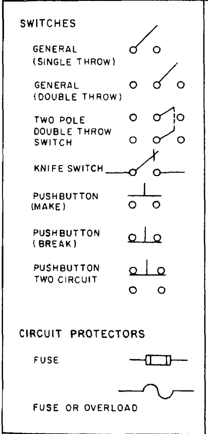
ZONE REFINING.—Technique of purifying a semiconductor or other substance by "sweeping" or passing a molten zone through the otherwise solid material.

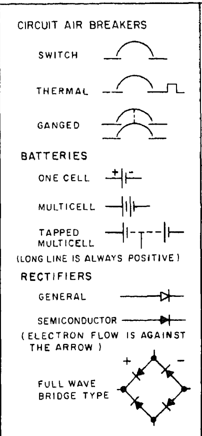
APPENDIX II

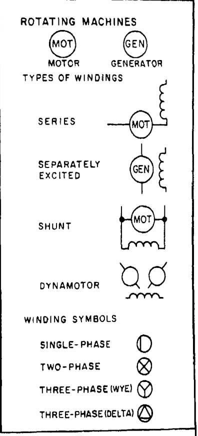
ELECTRICAL SYMBOLS


SHIPBOARD SYMBOLS
APPLIANCES; MISCELLANEOUS WIRING (GENERAL)
BOXES, GENERAL
BRANCH
CONNECTION
DISTRIBUTION
JUNCTION
BUS TRANSFER EQUIPMENT
NONAUTOMATIC OR PUSH BUTTON CONTROL
AC
DC
COMMUNICATION EQUIPMENT
BOX, SWITCH, TELEPHONE
JACKS
PLUGS, TELEPHONE
RECEPTACLE OR OUTLET
SWITCH
PUSH BUTTON
ON-OFF
SELECTOR
CIRCUIT LETTER
PANEL OR BULKHEAD
NUMBER OF SECTIONS
SNAP
TRANSFER
CONTROLLER, MOTOR (GENERAL)
C
BUILDUP EXAMPLES
CONTROLLER WITH LOW VOLTAGE RELEASE, RECLOSES UPON RETURN OF POWER
C LVR
CONTROLLER WITH LOW VOLTAGE PROTECTION, REMAINS OPEN UPON RETURN OF POWER
C LVP
FANS
FAN, PORTABLE BRACKET
F
FAN, OVERHEAD
F
HEATERS
HEATER, GENERAL
H
HEATER, PORTABLE RADIANT
H
LIGHTING UNITS
BULKHEAD
BULKHEAD, BERTH
HAND LANTERN
NAVIGATIONAL
NIGHT FLIGHT
OVERHEAD
PORTABLE
OVERHEAD, FLUORESCENT
GRAPHIC SYMBOLS
RESISTORS
OR
R1
GENERAL TAPPED
ADJUSTABLE TAP
CONTINUOUSLY VARIABLE
NONLINEAR
CAPACITORS
FIXED
VARIABLE
T
TRIMMER
GANGED
SHIELDED
SPLIT-STATOR
FEED-THROUGH
INDUCTIVE COMPONENTS
GENERAL
MAGNETIC CORE
TAPPED
ADJUSTABLE
ADJUSTABLE OR CONTINUOUSLY ADJUSTABLE
SATURABLE CORE REACTOR
TRANSFORMERS
GENERAL
MAGNETIC CORE TRANSFORMER
AUTOTRANSFORMER
WITH TAPS, SINGLE-PHASE

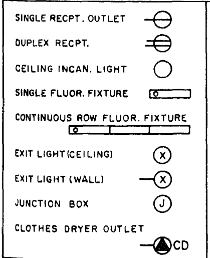
GRAPHIC SYMBOLS

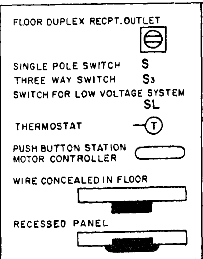


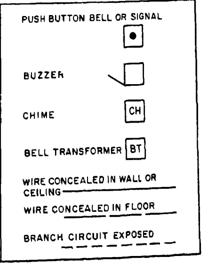




ARCHITECTURAL SYMBOLS




FLOOR DUPLEX RECPT. OUTLET
SINGLE POLE SWITCH
S
THREE WAY SWITCH
S3
SWITCH FOR LOW VOLTAGE SYSTEM
SL
THERMOSTAT
T
PUSH BUTTON STATION MOTOR CONTROLLER
WIRE CONCEALED IN FLOOR
RECESSED PANEL

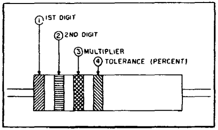


APPENDIX III

ELECTRONICS COLOR CODING

COLOR	1ST DIGIT	2ND DIGIT	MULTIPLIER	TOLERANCE (Percent)
Black	0	0	1	
Brown	1	1	10	
Red	2	2	100	
Orange	3	3	1,000	
Yellow	4	4	10,000	
Green	5	5	100,000	
Blue	6	6	1,000,000	
Violet	7	7	10,000,000	
Gray	8	8	100,000,000	
White	9	9	1,000,000,000	
Gold			.1	5
Silver			.01	10
No color				20

A



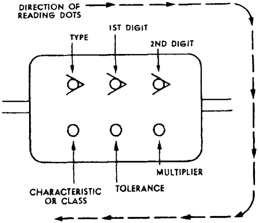
B

RESISTORS FOR MILITARY USE MAY HAVE A FIFTH BAND TO INDICATE RELIABILITY IN TERMS OF FAILURE RATE, AS FOLLOWS:

No Color: no test made
Brown : 1.0 percent per 100 hours
Red : 0.1 percent per 100 hours
Orange : 0.01 percent per 100 hours
Yellow : 0.001 percent per 100 hours

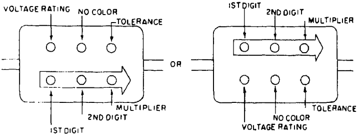
C

Resistor color code.



TYPE	COLOR	1ST DIGIT	2ND DIGIT	MULTIPLIER	TOLERANCE (PERCENT)	CHARACTERISTIC OR CLASS
JAN, MICA	BLACK	0	0	1.0		APPLIES TO TEMPERATURE COEFFICIENT OR METHODS OF TESTING
	BROWN	1	1	10	± 1	
	RED	2	2	100	± 2	
	ORANGE	3	3	1,000	± 3	
	YELLOW	4	4	10,000	± 4	
	GREEN	5	5	100,000	± 5	
	BLUE	6	6	1,000,000	± 6	
	VIOLET	7	7	10,000,000	± 7	
	GRAY	8	8	100,000,000	± 8	
EIA, MICA	WHITE	9	9	1,000,000,000	± 9	
	GOLD			.1	± 5	
	SILVER			.01	± 10	
	BODY				± 20	

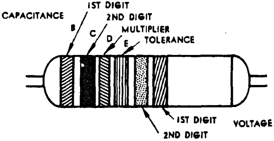
Dot color code for mica and molded paper capacitors.



COLOR	1ST DIGIT	2ND DIGIT	MULTIPLIER	TOLERANCE (PERCENT)	VOLTAGE RATING
BLACK	0	0	1 0		
BROWN	1	1	10	± 1	100
RED	2	2	100	± 2	200
ORANGE	3	3	1,000	± 3	300
YELLOW	4	4	10,000	± 4	400
GREEN	5	5	100,000	± 5	500
BLUE	6	6	1,000,000	± 6	600
VIOLET	7	7	10,000,000	± 7	700
GRAY	8	8	100,000,000	± 8	800
WHITE	9	9	1,000,000,000	± 9	900
GOLD			.1		1000
SILVER			.01	±10	2000
BODY				±20	*

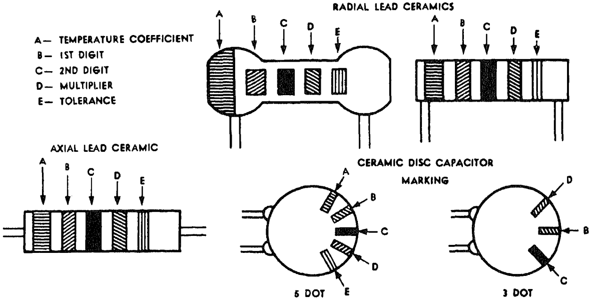
* WHERE NO COLOR IS INDICATED, THE VOLTAGE RATING MAY BE AS LOW AS 300 VOLTS.

Dot color code for capacitors (dielectric not specified).



COLOR	CAPACITANCE			TOLERANCE (PERCENT)	VOLTAGE RATING	
	1ST DIGIT	2ND DIGIT	MULTIPLIER		1ST DIGIT	2ND DIGIT
BLACK	0	0	1	±20	0	0
BROWN	1	1	10		1	1
RED	2	2	100		2	2
ORANGE	3	3	1,000	±30	3	3
YELLOW	4	4	10,000	±40	4	4
GREEN	5	5	100,000	± 5	5	5
BLUE	6	6	1,000,000		6	6
VIOLET	7	7			7	7
GRAY	8	8			8	8
WHITE	9	9		±10	9	9

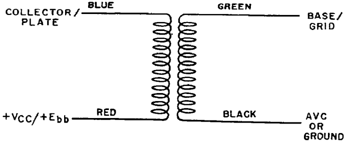
Band color code for tubular paper dielectric capacitors.



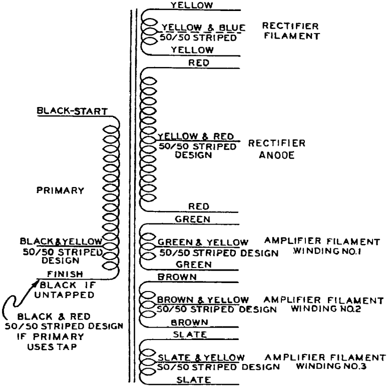
COLOR	1ST DIGIT	2ND DIGIT	MULTIPLIER	TOLERANCE		TEMPERATURE COEFFICIENT*
				MORE THAN 10 pf (IN PERCENT)	LESS THAN 10 pf (IN pf)	
BLACK	0	0	1.0	±20	±2.0	0
BROWN	1	1	10	± 1		−30
RED	2	2	100	± 2		−80
ORANGE	3	3	1,000			−150
YELLOW	4	4	10,000			−220
GREEN	5	5		± 5	±0.5	−330
BLUE	6	6				−470
VIOLET	7	7				−750
GRAY	8	8	.01		±0.25	+30
WHITE	9	9	.1	±10	±1.0	+120 TO −750 (EIA)
						+500 TO −330 (JAN)
SILVER						+100 (JAN)
GOLD						BYPASS OR COUPLING (EIA)

* PARTS PER MILLION PER DEGREE CELCIUS.

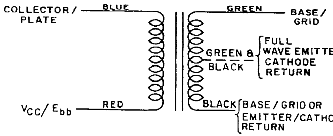
Color code for ceramic capacitors having different configurations.



IF TRANSFORMERS.


YELLOW
YELLOW & BLUE 50/50 STRIPED
RECTIFIER FILAMENT
YELLOW
RED
BLACK-START
YELLOW & RED 50/50 STRIPED DESIGN
RECTIFIER ANODE
PRIMARY
RED
GREEN
BLACK&YELLOW 50/50 STRIPED DESIGN
GREEN & YELLOW 50/50 STRIPED DESIGN
AMPLIFIER FILAMENT WINDING NO.1
GREEN
FINISH
BROWN
BLACK IF UNTAPPED
BROWN & YELLOW 50/50 STRIPED DESIGN
AMPLIFIER FILAMENT WINDING NO.2
BLACK & RED 50/50 STRIPED DESIGN IF PRIMARY USES TAP
BROWN
SLATE
SLATE & YELLOW 50/50 STRIPED DESIGN
AMPLIFIER FILAMENT WINDING NO.3
SLATE

POWER TRANSFORMERS.



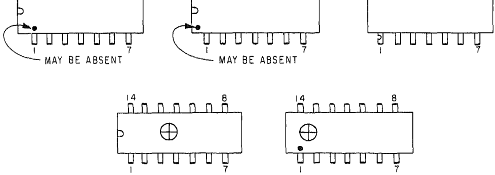
INTERSTAGE AUDIO TRANSFORMERS

STANDARD COLORS USED IN CHASSIS WIRING FOR TH PURPOSE OF CIRCUIT IDENTIFICATION OF THE EQUIPMEN ARE AS FOLLOWS:

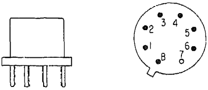
CIRCUIT	COLOR
GROUNDS, GROUNDED ELEMENTS, AND RETURNS	BLACK.
HEATERS OR FILAMENTS, OFF GROUND	BROWN.
POWER SUPPLY $+V_{CC}/+E_{bb}$	RED.
SCREEN GRIDS	ORANGE.
EMITTERS/CATHODES	YELLOW.
BASES/CONTROL GRIDS	GREEN.
COLLECTORS/ PLATES	BLUE
POWER SUPPLY, MINUS	VIOLET (PURPLE).
A.C. POWER LINES	GRAY.
MISCELLANEOUS, ABOVE OR BELOW GROUND RETURNS, AVC, ETC	WHITE.

FOR OTHER ELECTRICAL AND ELECTRONIC SYMBOLS REFER TO MILITARY STANDARD, MIL-STD-15-IA

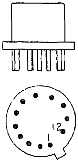
Color code for transformers.



TYPICAL DIP CONFIGURATION FOR LEAD NUMBERING
(14 LEAD CONFIGURATION FOR ILLUSTRATION PURPOSES ONLY)

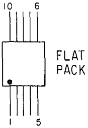


8-LEAD METAL CAN
10-LEAD SAME



12-LEAD METAL CAN

METAL CAN PACKAGE
TYPICAL LEAD CONFIGURATIONS



TYPICAL 10-LEAD FLAT PACKAGE LEAD CONFIGURATION

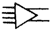
APPENDIX IV

ELECTRONICS SYMBOLS

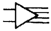
AMPLIFIER (2) *

GENERAL

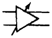
WITH TWO INPUTS



WITH TWO OUTPUTS

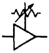


WITH ADJUSTABLE GAIN



WITH ASSOCIATED POWER SUPPLY

WITH ASSOCIATED ATTENUATOR



WITH EXTERNAL FEEDBACK PATH

AMPLIFIER LETTER COMBINATIONS (amplifier-use identification in symbol if required)

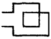
BDG	BRIDGING
BST	BOOSTER
CMP	COMPRESSION
DC	DIRECT CURRENT
EXP	EXPANSION
LIM	LIMITING
MON	MONITORING
PGM	PROGRAM
PRE	PRELIMINARY
PWR	POWER
TRQ	TORQUE

ANTENNA (3)

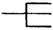
GENERAL

DIPOLE

LOOP

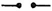


COUNTERPOISE



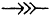
ARRESTER, LIGHTNING (4)

GENERAL

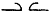


CARBON BLOCK

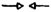
ELECTROLYTIC OR ALUMINUM CELL



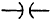
HORN GAP



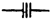
PROTECTIVE GAP



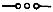
SPHERE GAP



VALVE OR FILM ELEMENT



MULTIGAP

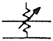


ATTENUATOR, FIXED (see PAD) (57)
(same symbol as variable attenuator, without variability)

ATTENUATOR, VARIABLE (5)

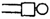
BALANCED

UNBALANCED



AUDIBLE SIGNALING DEVICE (6)

BELL, ELECTRICAL, RINGER, TELEPHONE



BUZZER

HORN, ELECTRICAL, LOUDSPEAKER, SIREN, UNDERWATER SOUND HYDROPHONE, PROJECTOR OR TRANSDUCER

HORN, LETTER COMBINATIONS (if required)

*HN	HORN, ELECTRICAL
*HW	HOWLER
*LS	LOUDSPEAKER
*SN	SIREN
†EM	ELECTROMAGNETIC WITH MOVING COIL
†EMN	ELECTROMAGNETIC WITH MOVING COIL AND NEUTRALIZING WINDING
†MG	MAGNETIC ARMATURE
†PM	PERMANENT MAGNET WITH MOVING COIL

(identification replaces (*) asterisk and (†) dagger)

SOUNDER, TELEGRAPH

BATTERY (7)

GENERALIZED DIRECT CURRENT SOURCE, ONE CELL

MULTICELL

CAPACITOR (8)

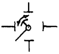
GENERAL

POLARIZED

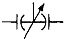
ADJUSTABLE OR VARIABLE

CONTINOUSLY ADJUSTABLE OR VARIABLE DIFFERENTIAL

PHASE-SHIFTER



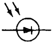
SPLIT-STATOR



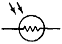
FEED-THROUGH

CELL, PHOTOSENSITIVE (Semiconductor) (9)

ASYMMETRICAL PHOTOCONDUCTIVE TRANSDUCER

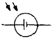


SYMMETRICAL PHOTOCONDUCTIVE TRANSDUCER



* NUMBER IN PARENTHESES INDICATES LOCATION OF SYMBOL IN MIL-STD PUBLICATION

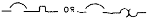
PHOTOVOLTAIC TRANSDUCER, SOLAR CELL



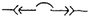
CIRCUIT BREAKER (11)

GENERAL

WITH MAGNETIC OVERLOAD



DRAWOUT TYPE



CIRCUIT ELEMENT (12)

GENERAL

CIRCUIT ELEMENT LETTER COMBINATIONS (replaces (*) asterisk)

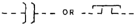
EG	EQUALIZER
FAX	FACSIMILE SET
FL	FILTER
FL-BE	FILTER, BAND ELIMINATION
FL-BP	FILTER, BAND PASS
FL-HP	FILTER, HIGH PASS
FL-LP	FILTER, LOW PASS
PS	POWER SUPPLY
RG	RECORDING UNIT
RU	REPRODUCING UNIT
DIAL	TELEPHONE DIAL
TEL	TELEPHONE STATION
TPR	TELEPRINTER
TTY	TELETYPEWRITER

ADDITIONAL LETTER COMBINATIONS (symbols preferred)

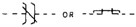
AR	AMPLIFIER
AT	ATTENUATOR
C	CAPACITOR
CB	CIRCUIT BREAKER
NS	HANDSET
I	INDICATING OR SWITCH BOARD LAMP
L	INDUCTOR
J	JACK
LS	LOUDSPEAKER
MIC	MICROPHONE
OSC	OSCILLATOR
PAD	PAD
P	PLUG
HT	RECEIVER, HEADSET
K	RELAY
R	RESISTOR
S	SWITCH OR KEY SWITCH
T	TRANSFORMER
WR	WALL RECEPTACLE

CLUTCH; BRAKE (14)

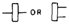
DISENGAGED WHEN OPERATING MEANS IS DE-ENERGIZED



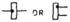
ENGAGED WHEN OPERATING MEANS IS DE-ENERGIZED



COIL, RELAY and OPERATING (16)

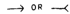


SEMICIRCULAR DOT INDICATES INNER END OF WIRING

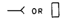


CONNECTOR (18)

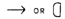
ASSEMBLY, MOVABLE OR STATIONARY PORTION; JACK, PLUG, OR RECEPTACLE



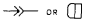
JACK OR RECEPTACLE



PLUG



SEPARABLE CONNECTORS

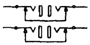


TWO-CONDUCTOR SWITCHBOARD JACK

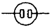
TWO-CONDUCTOR SWITCHBOARD PLUG

JACKS NORMALLED THROUGH ONE WAY

JACKS NORMALLED THROUGH BOTH WAYS

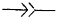


2-CONDUCTOR NONPOLARIZED, FEMALE CONTACTS



2-CONDUCTOR POLARIZED, MALE CONTACTS

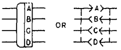
WAVEGUIDE FLANGE



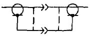
PLAIN, RECTANGULAR

CHOKE, RECTANGULAR

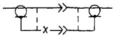
ENGAGED 4-CONDUCTOR, THE PLUG HAS 1 MALE AND 3 FEMALE CONTACTS, INDIVIDUAL CONTACT DESIGNATIONS SHOWN



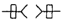
COAXIAL, OUTSIDE CONDUCTOR SHOWN CARRIED THROUGH



COAXIAL, CENTER CONDUCTOR SHOWN CARRIED THROUGH; OUTSIDE CONDUCTOR NOT CARRIED THROUGH



MATED CHOCK FLANGES IN RECTANGULAR WAVEGUIDE



COUNTER, ELECTROMAGNETIC; MESSAGE REGISTER (26)

GENERAL

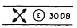
WITH A MAKE CONTACT

COUPLER, DIRECTIONAL (27)

(common coaxial/waveguide usage)

(common coaxial/waveguide usage)

E-PLANE APERTURE-COUPLING, 30-DECIBEL TRANSMISSION LOSS



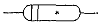
COUPLING (28)

BY LOOP FROM COAXIAL TO CIRCULAR WAVEGUIDE, DIRECT-CURRENT GROUNDS CONNECTED

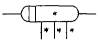
CRYSTAL, PIEZO-ELECTRIC (62)

DELAY LINE (31)

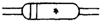
GENERAL



TAPPED DELAY

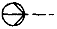


BIFILAR SLOW-WAVE STRUCTURE (commonly used in traveling-wave tubes)



(length of delay indication replaces (*) asterisk)

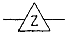
DETECTOR, PRIMARY; MEASURING TRANSDUCER (30) (see HALL GENERATOR and THERMAL CONVERTER)



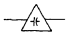
DISCONTINUITY (33)

(common coaxial/waveguide usage)

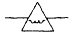
EQUIVALENT SERIES ELEMENT, GENERAL



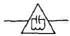
CAPACITIVE REACTANCE



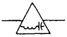
INDUCTIVE REACTANCE



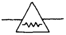
INDUCTANCE-CAPACITANCE CIRCUIT, INFINITE REACTANCE AT RESONANCE



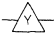
INDUCTANCE-CAPACITANCE CIRCUIT, ZERO REACTANCE AT RESONANCE



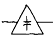
RESISTANCE



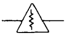
EQUIVALENT SHUNT ELEMENT, GENERAL



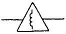
CAPACITIVE SUSCEPTANCE



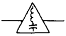
CONDUCTANCE



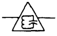
INDUCTIVE SUSCEPTANCE



INDUCTANCE-CAPACITANCE CIRCUIT, INFINITE SUSCEPTANCE AT RESONANCE

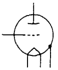


INDUCTANCE-CAPACITANCE CIRCUIT, ZERO SUSCEPTANCE AT RESONANCE

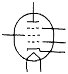


ELECTRON TUBE (34)

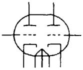
TRIODE



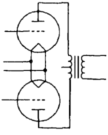
PENTODE, ENVELOPE CONNECTED TO BASE TERMINAL



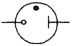
TWIN TRIODE, EQUIPOTENTIAL CATHODE



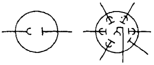
TYPICAL WIRING FIGURE TO SHOW TUBE SYMBOLS PLACED IN ANY CONVENIENT POSITION



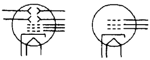
RECTIFIER, VOLTAGE REGULATOR
(see LAMP, GLOW)



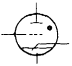
PHOTOTUBE, SINGLE AND MULTIPLIER



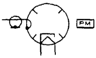
CATHODE-RAY TUBE, ELECTROSTATIC AND MAGNETIC DEFLECTION



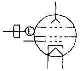
MERCURY-POOL TUBE, IGNITOR AND CONTROL GRID (see RECTIFIER)



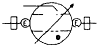
RESONANT MAGNETRON, COAXIAL OUTPUT AND PERMANENT MAGNET



REFLEX KLYSTRON, INTEGRAL CAVITY, APERTURE COUPLED

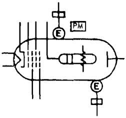


TRANSMIT-RECEIVE (TR) TUBE GAS FILLED, TUNABLE INTEGRAL CAVITY, APERTURE COUPLED, WITH STARTER



TRAVELING-WAVE TUBE (typical)

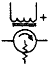
FORWARD-WAVE TRAVELING-WAVE-TUBE AMPLIFIER SHOWN WITH FOUR GRIDS, HAVING SLOW-WAVE STRUCTURE WITH ATTENUATION, MAGNETIC FOCUSING BY EXTERNAL PERMANENT MAGNET, rf INPUT AND rf OUTPUT COUPLING EACH E-PLANE APERTURE TO EXTERNAL RECTANGULAR



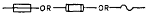
FERRITE DEVICES (100)

FIELD POLARIZATION ROTATOR

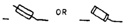
FIELD POLARIZATION AMPLITUDE MODULATOR



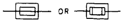
FUSE (36)



HIGH-VOLTAGE PRIMARY CUTOUT, DRY

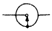


HIGH-VOLTAGE PRIMARY CUTOUT, OIL

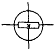


GOVERNOR (contact-making)
(37)

CONTACTS SHOWN HERE AS CLOSED

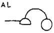


HALL GENERATOR (39)

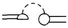


HANDSET (40)

GENERAL



OPERATOR'S SET WITH PUSH-TO-TALK SWITCH



HYBRID (41)

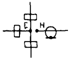
GENERAL

JUNCTION
(common coaxial/waveguide usage)

CIRCULAR

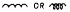
(E, H or HE transverse field indicators replace (*) asterisk)

RECTANGULAR WAVEGUIDE AND COAXIAL COUPLING



INDUCTOR (42)

GENERAL



IETIC CORE

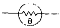
ED

STABLE. CONTINUOUSLY
STABLE

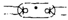
KEY, TELEGRAPH (43)

LAMP (44)

AST LAMP, BALLAST TUBE

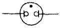


FLUORESCENT, 2 AND 4
NAL

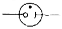


GLOW, NEON LAMP

A-C



D-C



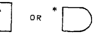
INCANDESCENT

TING LAMP; SWITCHBOARD

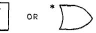
UAL SIGNALING DEVICE)

see 806B and Y32-14)
g some duplicate symbols,
right-hand symbols are not

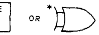
ction



ion



IVE-OR function



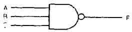
side of logic symbols in

CONDITION INDICATORS

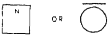
STATE (logic negation)

A LOGIC NEGATION OUTPUT BECOMES 1 STATE IF AND ONLY IF THE INPUT IS NOT 1 STATE

AN AND FUNC. WHERE OUTPUT IS LOW IF AND ONLY IF ALL INPUTS ARE HIGH

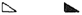


ELECTRIC INVERTER



(elec. invtr. output becomes 1-state if and only if the input is 1-state; elec. invtr. output is more pos. if and only if input is less pos.)

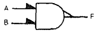
LEVEL (relative)



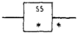
1 STATE IS LESS +	1-STATE IS MORE +

(symbol is a rt. triangle pointing in direction of flow)

AN AND FUNC. WITH INPUT 1-STATES AT MORE POS. LEVEL AND OUTPUT 1 STATE AT LESS POS. LEVEL

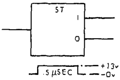


SINGLE SHOT (one output)

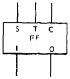


(waveform data replaces inside/outside (*))

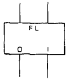
SCHMITT TRIGGER, WAVEFORM AND TWO OUTPUTS



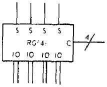
FLIP-FLOP, COMPLEMENTARY



FLIP-FLOP, LATCH

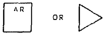


REGISTER



(binary register denoting four flip-flops and bits)

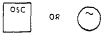
AMPLIFIER (see AMPLIFIER)



CHANNEL PATH(s) (see PATH, TRANSMISSION)

MAGNETIC HEADS (see PICK-UP HEAD)

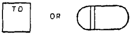
OSCILLATOR (see OSCILLATOR)



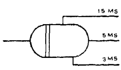
RELAY, CONTACTS (see CONTACT, ELECTRICAL) RELAY, ELECTROMAGNETIC (see RELAY COIL RECOGNITION

SIGNAL FLOW (see DIRECTION OF FLOW)

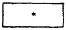
TIME DELAY (see DELAY LINE)



TIME DELAY WITH TYPICAL DELAY TAPS:



FUNCTIONS NOT OTHERWISE SYMBOLIZED



(identification replaces (*))

LOGIC LETTER COMBINATIONS

S	SET
C	CLEAR (reset)
T	TOGGLE (trigger)
(N)	NUMBER OF BITS
BO	BLOCKING OSCILLATOR
CF	CATHODE FOLLOWER
EF	EMITTER FOLLOWER
FF	FLIP-FLOP
SS	SINGLE SHOT
ST	SCHMITT TRIGGER
RG(N)	REGISTER (N stages)
SR	SHIFT REGISTER

MACHINE, ROTATING (46)

GENERATOR

MOTOR

METER, INSTRUMENT (48)

(identification replaces (*) asterisk)

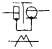
METER LETTER COMBINATIONS

A	AMMETER
AH	AMPERE-HOUR
CMA	CONTACT-MAKING (or breaking) AMMETER
CMC	CONTACT-MAKING (or breaking) CLOCK
CMV	CONTACT-MAKING (or breaking) VOLTMETER
CRO	OSCILLOSCOPE OR CATHODE-RAY OSCILLOGRAPH
DB	DB (decibel) METER
DBM	DBM (decibels referred to 1 milliwatt) METER
DM	DEMAND METER
DTR	DEMAND-TOTALIZING RELAY
F	FREQUENCY METER
G	GALVANOMETER
GD	GROUND DETECTOR
I	INDICATING
INT	INTEGRATING
µA or UA	MICROAMMETER
MA	MILLIAMMETER
NM	NOISE METER
OHM	OHMMETER
OP	OIL PRESSURE

MODE TRANSDUCER (53)

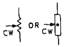
(common coaxial/waveguide usage)

TRANSDUCER FROM RECTANGULAR WAVEGUIDE TO COAXIAL WITH MODE SUPPRESSION, DIRECT-CURRENT GROUNDS CONNECTED



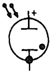
MOTION, MECHANICAL (54)

ROTATION APPLIED TO A RESISTOR



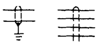
(identification replaces (*) asterisk)

NUCLEAR-RADIATION DETECTOR, GAS FILLED; IONIZATION CHAMBER; PROPORTIONAL COUNTER TUBE;
GEIGER-MULLER COUNTER TUBE (50) (see RADIATION-SENSITIVITY INDICATOR)



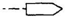
PATH, TRANSMISSION (58)

CABLE; 2-CONDUCTOR, SHIELD GROUNDED AND 5-CONDUCTOR SHIELDED

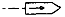


PICKUP HEAD (61)

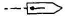
GENERAL



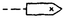
WRITING; RECORDING



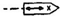
READING; PLAYBACK



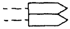
ERASING



WRITING, READING, AND ERASING



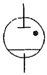
STEREO



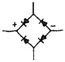
RECTIFIER (65)

SEMICONDUCTOR DIODE; METALLIC RECTIFIER; ELECTROLYTIC RECTIFIER; ASYMMETRICAL VARISTOR

MERCURY-POOL TUBE POWER RECTIFIER

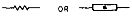


FULLWAVE BRIDGE-TYPE

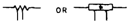


RESISTOR (68)

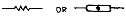
GENERAL



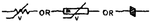
TAPPED



HEATING

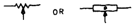


SYMMETRICAL VARISTOR RESISTOR, VOLTAGE SENSITIVE (silicon carbide, etc.)

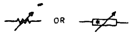


(Identification marks replace (*) asterisk)

WITH ADJUSTABLE CONTACT



ADJUSTABLE OR CONTINUOUSLY ADJUSTABLE (variable)

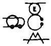


(Identification replaces (*) asterisk)

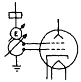
RESONATOR, TUNED CAVITY (71)

(common coaxial/waveguide usage)

RESONATOR WITH MODE SUPPRESSION COUPLED BY AN E-PLANE APERTURE TO A GUIDED TRANSMISSION PATH AND BY A LOOP TO A COAXIAL PATH

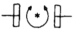


TUNABLE RESONATOR WITH DIRECT-CURRENT GROUND CONNECTED TO AN ELECTRON DEVICE AND ADJUSTABLY COUPLED BY AN E-PLANE APERTURE TO A RECTANGULAR WAVEGUIDE



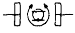
ROTARY JOINT, RF (COUPLER) (72)

GENERAL; WITH RECTANGULAR WAVEGUIDE

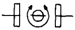


(transmission path recognition symbol replaces (*) asterisk)

COAXIAL TYPE IN RECTANGULAR WAVEGUIDE

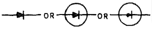


CIRCULAR WAVEGUIDE TYPE IN RECTANGULAR WAVEGUIDE

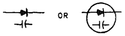


SEMICONDUCTOR DEVICE (73)
(Two Terminal, diode)

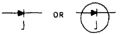
SEMICONDUCTOR DIODE; RECTIFIER



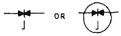
CAPACITIVE DIODE (also Varicap, Varactor, reactance diode, parametric diode)



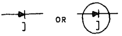
BREAKDOWN, DIODE, UNIDIRECTIONAL (also backward diode, avalanche diode, voltage regulator diode, Zener diode, voltage reference diode)



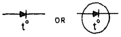
BREAKDOWN DIODE, BIDIRECTIONAL AND BACKWARD DIODE (also bipolar voltage limiter)



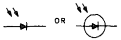
TUNNEL DIODE (also Esaki diode)



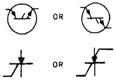
TEMPERATURE-DEPENDENT DIODE



PHOTODIODE (also solar cell)



SEMICONDUCTOR DIODE, PNPN SWITCH (also Shockley diode, four-layer diode and SCR).



(Multi-Terminal, transistor, etc.)

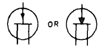
PNP TRANSISTOR

NPN TRANSISTOR

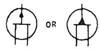
UNIJUNCTION TRANSISTOR, N-TYPE BASE

NIJUNCTION TRANSISTOR, P-
YPE BASE

ELD-EFFECT TRANSISTOR, N-
YPE BASE



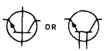
ELD-EFFECT TRANSISTOR, P-
PE BASE



MICONDUCTOR TRIODE, PNPN-
PE SWITCH

MICONDUCTOR TRIODE, NPNP-
PE SWITCH

N TRANSISTOR, TRANSVERSE-
ASED BASE



IP TRANSISTOR, OHMIC CON-
CTION TO THE INTRINSIC
GION

IN TRANSISTOR, OHMIC CON-
CTION TO THE INTRINSIC
GION

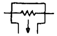
N TRANSISTOR, OHMIC CON-
CTION TO THE INTRINSIC
GION

P TRANSISTOR, OHMIC CON-
CTION TO THE INTRINSIC
GION

SQUIB (75)

EXPLOSIVE

IGNITER



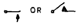
SENSING LINK, FUSIBLE LINK OPERATED

SWITCH (76)

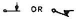
PUSH BUTTON, CIRCUIT CLOSING (make)

PUSH BUTTON, CIRCUIT OPENING (break)

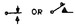
NONLOCKING, MOMENTARY CIRCUIT CLOSING (make)



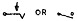
NONLOCKING; MOMENTARY CIRCUIT OPENING (break)



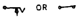
TRANSFER



LOCKING, CIRCUIT CLOSING (make)



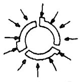
LOCKING, CIRCUIT OPENING (break)



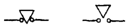
TRANSFER, 3-POSITION

WAFER

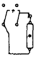
(example shown: 3-pole 3-circuit with 2 nonshorting and 1 shorting moving contacts)



SAFETY INTERLOCK, CIRCUIT OPENING AND CLOSING

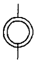


2-POLE FIELD-DISCHARGE KNIFE, WITH TERMINALS AND DISCHARGE RESISTOR



(identification replaces (*) asterisk)

SYNCHRO (78)

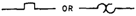


SYNCHRO LETTER COMBINATIONS

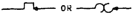
CDX	CONTROL-DIFFERENTIAL TRANSMITTER
CT	CONTROL TRANSFORMER
CX	CONTROL TRANSMITTER
TDR	TORQUE-DIFFERENTIAL RECEIVER
TDX	TORQUE-DIFFERENTIAL TRANSMITTER
TR	TORQUE RECEIVER
TX	TORQUE TRANSMITTER
RS	RESOLVER
B	OUTER WINDING ROTATABLE IN BEARINGS

THERMAL ELEMENT (83)

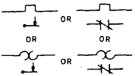
ACTUATING DEVICE



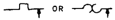
THERMAL CUTOUT; FLASHER



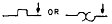
THERMAL RELAY



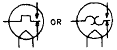
THERMOSTAT (operates on rising temperature), CONTACT



THERMOSTAT, MAKE CONTACT



THERMOSTAT, INTEGRAL HEATER AND TRANSFER CONTACTS



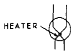
THERMISTOR; THERMAL RESISTOR (84)

WITH INTEGRAL HEATER

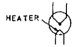
THERMOCOUPLE (85)

TEMPERATURE-MEASURING

CURRENT-MEASURING, INTEGRAL HEATER CONNECTED



CURRENT-MEASURING, INTEGRAL HEATER INSULATED

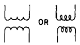


TEMPERATURE-MEASURING, SEMICONDUCTOR

CURRENT-MEASURING, SEMICONDUCTOR

TRANSFORMER (86)

GENERAL



MAGNETIC-CORE

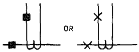
ONE WINDING WITH ADJUSTABLE INDUCTANCE

SEPARATELY ADJUSTABLE INDUCTANCE

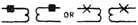
ADJUSTABLE MUTUAL INDUCTOR, CONSTANT-CURRENT

AUTOTRANSFORMER, 1-PHASE ADJUSTABLE

CURRENT, WITH POLARITY MARKING

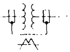


POTENTIAL, WITH POLARITY MARK



WITH DIRECT-CURRENT CONNECTIONS AND MODE SUPPRESSION BETWEEN TWO RECTANGULAR WAVEGUIDES

(common coaxial/waveguide usage)

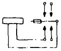


SHIELDED, WITH MAGNETIC CORE

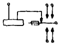
WITH A SHIELD BETWEEN WINDINGS, CONNECTED TO THE FRAME

VIBRATOR; INTERRUPTER (87)

TYPICAL SHUNT DRIVE (terminals shown)



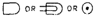
TYPICAL SEPARATE DRIVE (terminals shown)



VISUAL SIGNALING DEVICE (88)

COMMUNICATION SWITCHBOARD-TYPE LAMP

INDICATING, PILOT, SIGNALING, OR SWITCHBOARD LIGHT (see LAMP)



(identification replaces (*) asterisk)

INDICATING LIGHT LETTER COMBINATIONS

A	AMBER
B	BLUE
C	CLEAR
G	GREEN
NE	NEON
O	ORANGE
OP	OPALESCENT
P	PURPLE
R	RED
W	WHITE
Y	YELLOW

JEWELED SIGNAL LIGHT

APPENDIX V

GREEK ALPHABET

Name	Capital	Lower case	Designates
Alpha	Α	α	Angles.
Beta	Β	β	Angles, flux density.
Gamma	Γ	γ	Conductivity.
Delta	Δ	δ	Variation of a quantity, increment.
Epsilon	Ε	ϵ	Base of natural logarithms (2.71828).
Zeta	Ζ	ζ	Impedance, coefficients, coordinates.
Eta	Η	η	Hysteresis coefficient, efficiency.
Theta	Θ	θ	Phase angle.
Iota	Ι	ι	
Kappa	Κ	κ	Dielectric constant, coupling coefficient, susceptibility.
Lambda	Λ	λ	Wavelength.
Mu	Μ	μ	Permeability, micro, amplification factor.
Nu	Ν	ν	Reluctivity.
Xi	Ξ	ξ	
Omicon	Ο	ο	
Pi	Π	π	3.1416
Rho	Ρ	ρ	Resistivity.
Sigma	Σ	σ	Summation, standard deviation.
Tau	Τ	τ	Time constant, time-phase displacement.
Upsilon	Υ	υ	
Phi	Φ	ϕ	Angles, magnetic flux.
Chi	Χ	χ	
Psi	Ψ	ψ	Dielectric flux, phase difference.
Omega	Ω	ω	Ohms (capital), angular velocity (2 π f).

APPENDIX VI

FORMULAS

Ohm's Law for D-C circuits

$$I = \frac{E}{R} = \frac{P}{E} = \sqrt{\frac{P}{R}}$$

$$R = \frac{E}{I} = \frac{P}{I^2} = \frac{E^2}{P}$$

$$E = IR = \frac{P}{I} = \sqrt{PR}$$

$$P = EI = \frac{E^2}{R} = I^2R$$

Resistors in Series

$$R_T = R_1 + R_2 \dots$$

Resistors in Parallel

Two resistors

$$R_T = \frac{R_1 R_2}{R_1 + R_2}$$

More than two

$$\frac{1}{R_T} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \dots$$

Comparison of Units in Electric and Magnetic Circuits

	Electric circuit	Magnetic circuit
Force	Volt, E, or emf	Gilberts, F, or mmf.
Flow	Ampere, I	Flux, Φ, in maxwells.
Opposition	Ohms, R.	Reluctance, $\mathfrak{R}$.
Law	Ohms law, $I = \frac{E}{R}$	Rowland's law, $\Phi = \frac{F}{\mathfrak{R}}$.
Intensity of force	Volts per cm of length.	$H = \frac{1.257IN}{L}$, gilberts per centimeter of length.
Density	Current density--for example, amperes per cm^2.	Flux density--for example, lines per cm^2, or gausses.

R-L Circuit Time Constant equals

$$\frac{L \text{ (in henrys)}}{R \text{ (in ohms)}} = t \text{ (in seconds), or}$$

$$\frac{L \text{ (in microhenrys)}}{R \text{ (in ohms)}} = t \text{ (in microseconds)}$$

R-C Circuit Time Constants equals

R (ohms) × C (farads) = t (seconds)

R (megohms) × C (microfarads) = t (seconds)

R (ohms) × C (microfarads) = t (microseconds)

R (megohms) × C (micromicrofarads) = t (microseconds)

Capacitors in Series

Two capacitors

$$C_T = \frac{C_1 C_2}{C_1 + C_2}$$

More than two

$$\frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3} \dots$$

Capacitors in Parallel $C_T = C_1 + C_2 \dots$

Capacitive Reactance ($X_C = \frac{1}{2\pi fC}$)

Impedance in an R-C Circuit (Series)

$$Z = \sqrt{R^2 + X_C{}^2}$$

(No coupling between coils)

nductors in Parallel

Two inductors

$$L_T = \frac{L_1 L_2}{L_1 + L_2}$$

(No coupling between coils)

More than two

$$\frac{1}{L_T} = \frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3} \dots$$

(No coupling between coils)

Inductive Reactance

$$X_L = 2\pi f L$$

Q of a Coil

$$Q = \frac{X_L}{R}$$

Impedance of an R-L Circuit (Series)

$$Z = \sqrt{R^2 + X_L{}^2}$$

Impedance with R, C, and L in Series

$$Z = \sqrt{R^2 + (X_L - X_C)^2}$$

Parallel Circuit Impedance

$$Z = \frac{Z_1 Z_2}{Z_1 + Z_2}$$

Sine-Wave Voltage Relationships

Average value

$$E_{ave} = \frac{2}{\pi} \times E_{max} = 0.637 E_{max}$$

Effective or r.m.s. value

$$E_{eff} = \frac{E_{max}}{\sqrt{2}} = \frac{E_{max}}{1.414} = 0.707 E_{max} = 1.11 E_{ave}$$

Maximum value

$$E_{max} = \sqrt{2}\ E_{eff} = 1.414 E_{eff} = 1.57 E_{ave}$$

Voltage in an a-c circuit

$$E = IZ = \frac{P}{I \times P.F.}$$

Power in A-C Circuit

Apparent power = EI

True power (P = EI cos θ = EI × P.F.

Power Factor

$$P.F. = \frac{P}{EI} = \cos\theta$$

$$\cos\theta = \frac{\text{true power}}{\text{apparent power}}$$

Transformers

Voltage relationship

$$\frac{E_p}{E_s} = \frac{N_p}{N_s} \text{ or } E_s = E_p \times \frac{N_s}{N_p}$$

Current relationship

$$\frac{I_p}{I_s} = \frac{N_s}{N_p}$$

Induced voltage

$$E_{eff} = 4.44\ BAfN10^{-8}$$

Turns ratio equals

$$\frac{N_p}{N_s} = \sqrt{\frac{Z_p}{Z_s}}$$

Secondary current

$$I_s = I_p \frac{N_p}{N_s}$$

Secondary voltage

$$E_s = E_p \frac{N_s}{N_p}$$

Three-Phase Voltage and Current Relationships

With Wye connected windings

$$E_{line} = 1.732 E_{coil} = \sqrt{3}\ E_{coil}$$

$$I_{line} = I_{coil}$$

With delta connected windings

$$E_{line} = E_{coil}$$

$$I_{line} = 1.732 I_{coil}$$

With wye or delta connected winding

$$P_{coil} = E_{coil}\ I_{coil}$$

$$P_t = 3P_{coil}$$

$$P_t = 1.732E_{line}\ I_{line}$$

(To convert to true power multiply by $\cos\theta$)

Resonance

At resonance

$$X_L = X_C$$

Resonant frequency

$$F_o = \frac{1}{2\pi\sqrt{LC}}$$

Series resonance

$$Z \text{ (at any frequency)} = R + j(X_L - X_C)$$

$$Z \text{ (at resonance)} = R$$

Parallel resonance

$$A \text{ (at any frequency)} = \frac{Z_1 Z_2}{Z_1 + Z_2}$$

$$Z_{max} \text{ (at resonance)} = \frac{X_L X_C}{R} = \frac{X_L^2}{R} = QX_L = \frac{L}{CR}$$

Band width

$$\Delta = \frac{F_o}{Q} = \frac{R}{2\pi L}$$

Decibels

Power ratio

$$db = 10 \log_{10} \frac{P_2}{P_1}$$

Current and voltage ratio

$$db = 20 \log_{10} \frac{I_2\sqrt{R_2}}{I_1\sqrt{R_1}}$$

$$db = 20 \log_{10} \frac{E_2\sqrt{R_1}}{E_1\sqrt{R_2}}$$

NOTE: When R_1 and R_2 are equal they may be omitted from the formula.

When reference level is one milliwatt

$$dbm = 10 \log_{10} \frac{P}{0.001} \text{ (when P is in watts)}$$

Synchronous Speed of Motor

$$\text{r.p.m.} = \frac{120 \times \text{frequency}}{\text{number of poles}}$$

APPENDIX VII

LAWS OF EXPONENTS

Number	Powers of Ten	Prefix	Symbol
1,000,000,000,000 =	10^{12}	Tera	T
1,000,000,000 =	10^9	Giga	G
1,000,000 =	10^6	Mega	M
100,000 =	10^5		
10,000 =	10^4		
1,000 =	10^3	Kilo	k
100 =	10^2	Hecto	h
10 =	10^1	Deka	dk
1 =	10^0		
0.1 =	10^{-1}	Deci	d
0.01 =	10^{-2}	Centi	c
0.001 =	10^{-3}	Milli	m
0.0001 =	10^{-4}		
0.00001 =	10^{-5}		
0.000001 =	10^{-6}	Micro	μ
0.000000001 =	10^{-9}	Nano	n
0.000000000001 =	10^{-12}	Pico	p

To multiply like (with same base) exponential quantities, add the exponents. In the language of algebra the rule is $a^m \times a^n = a^{m+n}$.

$$10^4 + 10^2 = 10^{4+2} = 10^6$$

$$0.003 \times 825.2 = 3 \times 10^{-3} \times 8.252 \times 10^2 =$$

$$24.756 \times 10^{-1} = 2.4756$$

To divide like exponential quantities, subtract the exponents. In the language of algebra the rule is

$$\frac{a^m}{a^n} = a^{m-n} \text{ or } 10^8 + 10^2 = 10^6$$

$$3,000 + 0.015 = (3 \times 10^3) + (1.5 \times 10^{-2}) =$$

$$2 \times 10^5 = 200,000$$

$$(10^3)^4 = 10^{3 \times 4} = 10^{12}$$

$$2,500^2 = (2.5 \times 10^3) = 6.25 \times 10^6 =$$
$$6,250,000$$

Any number (except zero) raised to the zero power is one. In the language of algebra $x^0 = 1$

$$x^3 \div x^3 = 1$$

$$10^4 \div 10^4 = 1$$

Any base with a negative exponent is equal to 1 divided by the base with an equal positive exponent. In the language of algebra

$$x^{-a} = \frac{1}{x^a}$$

$$10^{-2} = \frac{1}{10^2} = \frac{1}{100}$$

$$5a^{-3} = \frac{5}{a^3}$$

$$(6a)^{-1} = \frac{1}{6a}$$

To raise a product to a power, raise each factor of the product to that power.

$$(2 \times 10)^2 = 2^2 \times 10^2$$

$$3,000^3 = (3 \times 10^3)^3 = 27 \times 10^9$$

To find the nth root of an exponential quantity, divide the exponent by the index of the root. Thus, with nth root of $a^m = a^{m/n}$.

$$\sqrt{x^6} = x^{6/2} = x$$

$$\sqrt[3]{64 \times 10^3} = 4 \times 10 = 40$$

APPENDIX VIII

THE METRIC SYSTEM

MEASURES OF LENGTH

Metric denominations and values		Equivalents in denominations in use	
Myriameter	10,000 meters	6.2137	miles.
Kilometer	1,000 meters	0.62137	mile, or 3,280 feet and 10 inches.
Hectometer	100 meters	328	feet and 1 inch.
Dekameter	10 meters	393.7	inches.
Meter	1 meter	39.37	inches.
Decimeter	1/10 of a meter	3.937	inches.
Centimeter	1/100 of a meter	0.3937	inch.
Millimeter	1/1000 of a meter	0.0394	inch.

MEASURES OF CAPACITY

Metric denominations and values			Equivalents in denominations in use	
Names	Number of liters	Cubic measure	Dry measure	Liquid or wine measure
Kiloliter or stere	1,000	1 cubic meter	1.308 cubic yards	264.17 gallons.
Hectoliter	100	1/10 of a cubic meter	2 bushels and 3.35 pecks	26.417 gallons.
Dekaliter	10	10 cubic decimeters	9.08 quarts	2.6417 gallons.
Liter	1	1 cubic decimeter	0.908 quart	1.0567 quarts.
Deciliter	1/10	1/10 of a cubic decimeter	6.1022 cubic inches	0.845 gill.
Centiliter	1/100	10 cubic centimeters	0.6102 cubic inch	0.338 fluid ounce.
Milliliter	1/1000	1 cubic centimeter	0.061 cubic inch	0.27 fluid dram.

MEASURES OF SURFACE

Metric denominations and values		Equivalents in denominations in use	
Hectare	10,000 square meters	2.471	acres.
Are	100 square meters	119.6	square yards.
Centare	1 square meter	1,550	square inches.

WEIGHTS

Metric denominations and values			Equivalents in denominations in use
Names	Number of grams	Weight of what quantity of water at maximum density	Avoirdupois weight
Millier or tonneau	1,000,000	1 cubic meter	2204.6 pounds.
Quintal	100,000	1 hectoliter	220.46 pounds.
Myriagram	10,000	10 liters	22.046 pounds.
Kilogram or kilo	1,000	1 liter	2.2046 pounds.
Hectogram	100	1 deciliter	3.5274 ounces.
Dekagram	10	10 cubic centimeters	0.3527 ounce.
Gram	1	1 cubic centimeter	15.432 grains.
Decigram	1/10	1/10 of a cubic centimeter	1.5432 grains.
Centigram	1/100	10 cubic millimeters	0.1543 grain.
Milligram	1/1000	1 cubic millimeter	0.0154 grain.

APPENDIX IX

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HOW TO COMPLETE THIS COURSE SUCCESSFULLY

You should study the RTM before attempting to answer the questions in the course. The RTM pages that you are to study are listed at the beginning of each assignment. Pay close attention to tables and illustrations as they contain information which will help you to understand the text. You should read the learning objectives provided in the text at the beginning of each chapter or topic or in the course preceding each set of questions. The learning objectives tell you what you should be able to do after studying the RTM. Answering the questions correctly should help you accomplish the objectives.

After studying the text, you should be ready to answer the questions in the assignment. Read each question carefully. Select the BEST ANSWER for each question based on your understanding of the content of the RTM. You may discuss difficult points in the course with others. However, the answer you select must be your own.

Using the appropriate answer sheet, write in the proper assignment number. Ensure the heading information is correctly filled out on the conventional answer sheets, which are located in the back of the course. In the case of the Automatic Data Processing (ADP) answer sheet, be sure that the information is correctly entered in the appropriate spaces.

You are prohibited from referring to or copying the solutions of others and from giving completed solutions or answers to anyone else. Noncompliance can result in suspension from the course by the administering activity and disciplinary action by Commander, Naval Military Personnel Command.

LOCAL COMMAND

As you finish each assignment, submit the completed answer sheet to your ESO for grading. The graded answer sheet will not be returned to you.

After you submit all required answer sheets and achieve at least a 3.2 grade on each assignment, your command will make the necessary entry in your service record, giving you credit for your work. Letters of satisfactory completion are not issued by the Naval Education and Training Program Development Center for courses administered by local commands.

If you are completing this NRCC to become eligible to take an advancement examination, be sure to follow a schedule that will enable you to complete all assignments on time. Your schedule should call for the completion of at least one assignment per month.

WHEN YOUR COURSE IS ADMINISTERED BY THE NAVAL EDUCATION AND TRAINING PROGRAM DEVELOPMENT CENTER

If this course will be administrated by the Naval Education and Training Program Development Center, you will be provided ADP answer sheets to submit in lieu of the conventional answer sheets contained in the back of this course. The ADP answer sheets must be used and may not be duplicated.

Your answer sheets will not be returned. However, you will be notified which questions were missed. In the event your score is less than 3.2 for an assignment, you will be sent a resubmit answer sheet to complete.

As you complete each assignment, mail the completed ADP answer sheet to the Naval Education and Training Program Development Center where it will be graded. Make sure all the required information on each ADP answer sheet is filled in. Unless you furnish all the information required, you may not receive credit for your work.

Program Development Center will issue you a letter of satisfactory completion to certify successful completion of the course (or a creditable unit of the course). To receive a course completion letter, follow the directions given on the Course Completion form in the back of this NRCC.

NOTE: DO NOT USE THE COURSE COMMENTS PAGE AS THE ENVELOPE FOR RETURNING ANSWER SHEETS OR COURSE MATERIALS.

Envelopes and packing materials for returning answer sheets and course materials should be obtained locally.

RETURN YOUR ADP ANSWER SHEETS TO:

Commanding Officer
Naval Education and Training Program
Development Center, Code 324
Pensacola, FL 32559-5000

Questions concerning the courses administered by NAVEDTRAPRODEVCEN should be referred to the above address or by telephone: AUTOVON 922-1343, FTS 948-1343, or commercial (904) 452-1343.

NAVAL RESERVE RETIREMENT CREDIT

This course is evaluated at 5 Naval Reserve retirements points. These points are creditable to personnel eligible to receive them under current directives governing retirement of Navy Reserve personnel.

COURSE OBJECTIVES

In completing this NRCC, you will demonstrate a knowledge of the subject matter by correctly answering questions on the following: The evolution of computing devices, types of computers and their analytical processes, electronic theories of modern day computers, AN/UYK-20 computer, Synchronous Distributed Processor, AN/UYK-7 computer, Super Bee computer terminal, TermiNet 1200 printer, AN/USH-26 recorder-reproducer, Asynchronous Channel Multiplexer, Input Processor Unit 1-1, Power Supply Units 26-1, 2, and 3, Model 40 teletypewriter, Disk Storage Systems, and CDC 9766 Storage Module Drives.

the type of each question, and the action required, by inspection of the samples given below.

MULTIPLE-CHOICE QUESTIONS

question contains several alternatives, one of which provides the best answer to the question. Select the rnative, and blacken the appropriate box on the answer sheet.

SAMPLE

ho was the first person appointed
cretary of Defense under the
tional Security Act of 1947?

George Marshall
James Forrestal
Chester Nimitz
William Halsey

Indicate in this way on the answer sheet:

	1 T	2 F	3	4	
s-1	☐	■	☐	☐	_ _ _

TRUE-FALSE QUESTIONS

each statement true or false as indicated below. If any part of the statement is false the statement is to dered false. Make the decision, and blacken the appropriate box on the answer sheet.

SAMPLE

l naval officers are authorized to rrespond officially with any systems mmand of the Department of the vy without their respective commnding officer's endorsement.

True
False

Indicate in this way on the answer sheet:

	1 T	2 F	3	4	
s-2	☐	■	☐	☐	_ _ _

MATCHING QUESTIONS

set of questions consists of two columns, each listing words, phrases or sentences. The task is to select in column B which is the best match for the item in column A that is being considered. Items in column e used once, more than once, or not at all. Specific instructions are given with each set of questions. Select bers identifying the answers and blacken the appropriate boxes on the answer sheet.

SAMPLE

estions s-3 through s-6, match the name of the shipboard officer in column A by selecting from column me of the department in which the officer functions. Some responses may be used once, more than once, t all.

A. OFFICER	B. DEPARTMENT
nage Control Assistant	1. Operations Department
: Officer	2. Engineering Department
oursing Officer	3. Supply Department
nmunications Officer	

Indicate in this way on the answer sheet:

	1 T	2 F	3	4	
s-3	☐	■	☐	☐	_ _ _
s-4	■	☐	☐	☐	_ _ _
s-5	☐	☐	■	☐	_ _ _
s-6	■	☐	☐	☐	_ _ _

Assignment 1

book Assignment: "Introduction to Computers." Pages 1-1 through 1-39.

In this course you will demonstrate that learning has taken place by correctly answering ning items. The mere physical act of indicating a choice on an answer sheet is not in itself rtant; it is the mental achievement, in whatever form it may take, prior to the physical act is important and toward which course learning objectives are directed. The selection of the ect choice for a course training item indicates that you have fulfilled, at least in part, stated objective(s).

The accomplishment of certain objectives, for example, a physical act such as drafting a , cannot readily be determined by means of objective type course items; however, you can nstrate by means of answers to training items that you have acquired the requisite knowledge erform the physical act. The accomplishment of certain other learning objectives, for ple, the mental acts of comparing, recognizing, evaluating, choosing, selecting, etc., may eadily demonstrated in a course by indicating the correct answers to training items.

The comprehensive objective for this course has already been given. It states the purpose he course in terms of what you will be able to do as you complete the course.

The detailed objectives in each assignment state what you should accomplish as you progress ugh the course. They may appear singly or in clusters of closely related objectives, as opriate; they are followed by items which will enable you to indicate your accomplishment.

All objectives in this course are learning objectives and items are teaching items. They out important things, they assist in learning, and they should enable you to do a better or the Navy.

This self-study course is only one part of the total Navy training program; by its very e it can take you only part of the way to a training goal. Practical experience, schools, cted reading, and the desire to accomplish are also necessary to round out a fully meaningful ning program.

Learning Objective: Describe the evolution of the computer and identify the persons involved in its development.

Early man used which of the following devices as an aid to counting?

1. Fingers
2. Stones and pebbles
3. Both 1 and 2 above
4. The calculus

1-2. The use of different colors or shapes of stones for the representation of certain values evolved into which of the following systems?

1. Calendar systems
2. Astronomy systems
3. Monetary systems
4. Geometric systems

1-3. What name was given to the early static storage device for the progressive results of decimal calculation?

1. Compiler
2. Abacu
3. Dice
4. Calculator

NVENTION IN COLUMN A. RESPONSES MAY BE USED
ORE THAN ONCE.

A. INVENTION	B. INVENTOR
1-4. A type of mechanical adding machine in 1642	1. John Thomas
	2. Charles Babbage
1-5. A commercially successful calculator in 1820	3. Blaise Pascal
	4. Herman Hollerith
1-6. The difference engine	
1-7. Machines that could evaluate information from punched cards	
1-8. The analytical engine	

1-9. The differential analyzer was used as a navigation aid during the Civil War.

1. True
2. False

-10. The Harvard Mark I was the first fully automatic data processing system.

1. True
2. False

Learning Objective: Identify the types of software used in computers.

-11. Which of the following items are NOT considered to be computer software?

1. Microchips
2. Compilers
3. Assemblers
4. Execution routines

PERFORMED BY THE PROGRAMMING LANGUAGE LISTED IN COLUMN A. NOT ALL RESPONSES IN COLUMN B ARE USED.

A. COMPUTER LANGUAGE	B. FUNCTION
1-12. FORTRAN	1. Used in micro computers only
1-13. PL/1	
1-14. Jovial	2. Used for real-time applications
	3. Used for business and scientific applications
	4. Used for large-scale command and control systems

Learning Objective: Describe the types of computers and their analytical processes.

1-15. What are the two basic types of computers?

1. Linear and digital
2. Analog and digital
3. Binary and logic
4. Linear and octal

1-16. As it applies to computers, what does the term analog mean?

1. Representation by means of continuously variable physical quantities
2. Representation by the use of numerical equivalents
3. Representation by the use of graphic analysis
4. Representation by the SWAG

1-17. Analog computers, because of their design, have unlimited applications.

1. True
2. False

1-18. What method is used to represent the instructions used by a digital computer?

1. Analog input
2. Delayed transmission
3. Numerical equivalents
4. Direct translation

operation of a special-purpose digital computer?

1. The input frequency must be increased
2. The primary RTMS must be altered
3. The software must be changed
4. The construction of the machine must be altered

A register is a series of electronic devices for the permanent storage of a binary word.

1. True
2. False

Devices used to control the transfer of data words from one register to another are known as

1. gates
2. RAMs
3. LEDs
4. ROMs

Learning Objective: Identify the elements of a digital computer and describe their purpose.

ISWERING QUESTIONS 1-22 THROUGH 1-24,
T THE FUNCTION FROM COLUMN B WHICH IS
RMED BY THE UNIT LISTED IN COLUMN A. NOT
ESPONSES IN COLUMN B ARE USED.

A. UNIT	B. FUNCTION
Control unit	1. Performs the actual processing
Arithmetic-logic unit	2. Stores the data to be processed
Internal data storage unit	3. Used for the input of data
	4. Directs the overall operation of the computer

In the control unit of a typical digital computer, what does the "P" register contain?

1. The address of the instruction being executed
2. The instruction word during execution
3. The address of the next instruction to be executed
4. The quantity used for address modification

into what four general categories?

1. Transfer, arithmetic, logic, and control
2. Bit, byte, digit, and literal
3. Input, output, shift, and double
4. Binary, octal, digital, and hexadecimal

1-27. Instructions that provide the computer with the ability to make decisions based on the results of previously generated data are known by what name?

1. Logic instructions
2. Control instructions
3. Division instruction
4. Arithmetic instructions

1-28. Arithmetic and logic operations are performed in what section of a digital computer?

1. RAM
2. I/O
3. CPU
4. ALU

1-29. What is the purpose of "bootstrap" instructions?

1. To cause the program to "branch" depending on whether a certain condition is met
2. To place enough instructions into a computer memory so that these instructions can be used to bring in more instructions
3. To cause the program to terminate if a "bad-data" input is sensed
4. To perform multiplication of certain numbers

1-30. Which of the following are used as memory storage devices?

1. Magnetic cores
2. Semiconductors
3. Thin film
4. All of the above

1-31. In magnetic core memories, a single core can store how many bits of a word?

1. One
2. Two
3. Three
4. Four

in modern digital computers are of what type?

1. ROM MSI
2. RAM SSI
3. MOS LSI
4. NIS NSI

IN ANSWERING QUESTIONS 1-33 THROUGH 1-35, SELECT THE STORAGE DEVICE FROM COLUMN B WHICH IS DESCRIBED IN COLUMN A. NOT EVERY RESPONSE IN COLUMN B IS USED

	A. DESCRIPTION	B. STORAGE DEVICE
1-33.	Arranged in arrays to assign memory address locations and to quickly write or locate data for read-out purposes	1. Magnetic film 2. Magnetic drum 3. Magnetic core 4. Magnetic tape
1-34.	Large storage capacity and low cost, but requires long access time to locate data which is widely distributed along the storage device	
1-35.	Uses a number of read and write heads for recording and reading. All data stored on this storage device is referenced to a reference pulse	

1-36. What is/are the general form(s) of input data to a computer?

1. Manual inputs from a man-machine interface (MMI) such as a keyboard or console
2. Analog inputs from instruments or sensors
3. Inputs from a source on or in which data has previously been stored in a form intelligible to the computer
4. All of the above

ally takes which of the following forms?

1. Codes or symbols displayed on a cathode ray screen or other device
2. Manually generated control information
3. Information recorded in ROM
4. Software documentation

1-38. Which of the following is a common limitation of most input devices?

1. They involve some mechanical operation
2. They are located a great distance from the computer
3. They require single-phase power
4. They are not compatible with the computer

Learning Objective: Identify the electronic elements in a digital computer and describe their theory of operation.

IN ANSWERING QUESTIONS 1-39 THROUGH 1-41, SELECT FROM COLUMN B THE DESCRIPTION THAT MATCHES THE DEVICE IN COLUMN A. NOT EVERY RESPONSE IN COLUMN B IS USED.

	A. DEVICE	B. DESCRIPTION
1-39.	SSI	1. Twelve or more circuits, equivalent in complexity to a typical logic gate
1-40.	MSI	2. Fewer than 10 circuits, no more complex than a typical logic gate
1-41.	VLSI	3. Large and complex circuitry, equivalent to 100 or more logic gates
		4. Contains the equivalent of 1000 or more logic gates

1-42. A three-state TTL circuit can be used in which of the following ways?

1. In core memory construction
2. In bus oriented digital circuit designs
3. As a power supply
4. As a filter circuit

operation?

1. High power dissipation
2. Interconnections between circuits must be short
3. Close circuit spacing creates packaging difficulties
4. Each of the above

What type of logic circuit was developed to permit the construction of large, complex LSI bipolar circuits?

1. IIL
2. T^2L
3. ITL
4. ECL

IN ANSWERING QUESTION 1-45 REFER TO FIGURE 1-14 AND THE APPROPRIATE SECTION UR RTM.

When will Q1 be cut off?

1. When the input is in the low state
2. When the input is in the high state
3. When the current from Q2 is supplied to the base of Q1
4. When the collector of Q1 is at the low state or near ground

IN ANSWERING QUESTIONS 1-46 AND 1-47, REFER TO FIGURE 1-15 AND THE APPROPRIATE ON IN YOUR RTM.

Under which of the following conditions will Q3 be cut off?

1. When both A and B are high
2. When A is low and B is high
3. When A is high and B is low
4. Both 2 and 3 above

With Q3 cut off what will be the condition of "C"?

1. Low
2. High
3. At ground potential

An improvement in the switching speeds of I^2L circuits can be achieved by the addition of which of the following devices?

1. Blocking resistors
2. Zenner diodes
3. Electrolyte capacitors
4. Schottky diodes

1. T^2L
2. NTL
3. FET
4. GPT

1-50. An n-channel enhancement mode MOSFET consists of (a) what two types of semiconductor areas fused into (b) what type of substrate?

1. (a) P-type (b) n-type
2. (a) N-type (b) a-type
3. (a) N-type (b) p-type
4. (a) N-type (b) nonconducting

IN ANSWERING QUESTIONS 1-51 AND 1-52, REFER TO FIGURE 1-16 AND THE APPROPRIATE SECTION IN YOUR RTM.

1-51. When the voltage difference between the source and the gate is zero, what is the conduction state of the MOSFET illustrated?

1. Nonconducting
2. Conducting at less than saturation
3. Conducting at saturation
4. Conducting at cutoff

1-52. Which, if any, of the following conditions will cause gate current to flow in the MOSFET illustrated?

1. When the gate is made positive with respect to the source
2. When the gate is made negative with respect to the source
3. When the source and drain are at equal potentials
4. None of the above

IN ANSWERING QUESTION 1-53, REFER TO FIGURE 1-17 AND THE APPROPRIATE SECTION IN YOUR RTM.

1-53. The device in view B has what type of substrate?

1. PN
2. P
3. N
4. NP

IN ANSWERING QUESTION 1-54, REFER TO FIGURE 1-18 AND THE APPROPRIATE SECTION IN YOUR RTM.

1-54. What is the purpose of Q2 in view B?

1. To act as a small resistance value
2. To act as a large resistancc value
3. To isolate dc voltages
4. To reduce oscillations

transistors?

1. JFET
2. CMOS
3. AMOS
4. IGFET

-56. What is the primary disadvantage of CMOS devices?

1. Their large size
2. Power consumption
3. Operating frequency
4. Voltage requirements

-57. What is the reason for the relatively slow speed of a MOSFET?

1. Voltage requirements
2. Size
3. Low impedance
4. High impedance

-58. The control section of a digital computer serves what purpose(s)?

1. To provide for input and output of data and to control signals
2. To store the operational program and provide additional routine storage
3. To interpret the program stored in memory and generate control signals
4. To provide power and address modification

Learning Objective: Identify the functions of the control section in a digital computer.

-59. The outputs of the instruction decoder and various timing pulses are combined in the program counter to form the desired control signals.

1. True
2. False

-60. What is the main element of a microprogram control unit?

1. A ROM
2. A RAM
3. A PRAM
4. A SAM

1. macroinstructions
2. machoinstructions
3. miniinstructions
4. microinstructions

IN ANSWERING QUESTIONS 1-62 AND 1-63, REFER TO FIGURE 1-23 (VIEW B) AND THE APPROPRIATE SECTION IN YOUR RTM.

1-62. The ROM address register receives its input from how many sources?

1. One
2. Two
3. Three
4. Four

1-63. What entity effectively defines the start address for a microprogram that will generate control pulses to carry out a particular instruction?

1. Op-code from the IR
2. Miniinstruction
3. Destination code from SU
4. Op-code from the ARU

1-64. When the ROM in the microprogram controller is replaceable, what advantage is gained?

1. The ALU of the computer is expanded
2. Many different instruction sets can be used with the computer
3. The physical size of main memory may be increased
4. The I/O section of the computer can be altered

1-65. Which of the following is a technique that is used to minimize the impact of changing from one computer system to another?

1. Ramification
2. Edification
3. Emulation
4. Interpretation

1-66. Which of the following is a disadvantage of a ROM microprogram control unit?

1. Large physical size
2. Relative lack of speed
3. High failure rate
4. Lack of flexibility

SECTION IN YOUR RTM.

1-67. What is the purpose of the inverters at the input side of the circuit?

1. To act as switching circuits
2. To convert digital data to analog
3. To convert analog data to digital
4. To buffer the binary bits and generate the complements

1-68. How can you configure the PLA outputs so that the normal or complement output is realized?

1. By using dropping resistors and varistors between the AND gates and the OR gates
2. By using tri-state NOR gates wired in series with a cophase amplifier
3. By programming the presence or absence of an inverter at each output point
4. By reversing the leads on the OR gates

1-69. Most of the data processing functions are carried out in what part of a digital computer?

1. 1/O section
2. Arithmetic-logic section
3. Main memory
4. Memory interfacing unit

Learning Objective: Demonstrate a basic familiarity with computer memories. (This objective is continued in assignment 2.)

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core memory?

1. The intensity of the magnetic field around a core
2. The absence or presence of a magnetic charge
3. The direction of the magnetic field on the core
4. The temperature of the core aperature

1-71. What term is used to describe a computer memory that loses data storage if power is removed?

1. Permeability
2. Nonvolatility
3. Volatility
4. Retainability

1-72. What are the two basic types of semiconductor memories used in digital computers?

1. EPROM and REM
2. RAM and ROM
3. REM and ROM
4. SAM and ROM

1-73. In what type of memory is data written into the memory at time of manufacture and cannot be changed?

1. Random access memory
2. Read/write memory
3. Both 1 and 2 above
4. Read-only memory

1-74. RAM and ROM memories have what type of memory access?

1. Sequential
2. Parallel
3. Random
4. End around

Assignment 2

Textbook Assignment: "Introduction to Computers" (Continued). Pages 1-39 through 1-78.

Learning Objective (Continued): Demonstrate a basic familiarity with computer memories.

2-1. Which of the following definitions most closely defines "access time" for a write operation?

1. From the time when data is presented to the memory to the time that it is actually stored
2. From the time when data is entered at an MMI device to the time it is actually stored
3. From the time when data is presented to the memory to the time it is read back from the memory
4. From the time when data is requested from memory to the time it is actually at the memory output

2-2. Basic semiconductor memories are broken down into storage cells. How many bits of data can be stored in each storage cell?

1. One
2. Two
3. Three
4. Four

2-3. How many maximum memory locations can be accessed by a 7-bit address word?

1. 64
2. 128
3. 256
4. 512

2-4. Using the shorthand method in describing memory systems, how should you refer to a memory with 32,768 memory locations?

1. 32K
2. 33K
3. 32.7K
4. 32.77K

2-5. A memory organized to accommodate 256 four-bit words (1024 bits) requires an address of how many bits in order to access all of the memory?

1. 7
2. 8
3. 9
4. 10

Learning Objective: Identify the characteristics of dynamic semiconductor memories.

2-6. Which of the following is a disadvantage of static semiconductor memories as compared to dynamic semiconductor memories?

1. High cost per bit
2. Relatively large size
3. High power consumption
4. Each of the above

2-7. Which of the following are disadvantages of dynamic semiconductor memories?

1. High cost and power consumption
2. Cooling requirements and disposition to fail
3. Complexity and critical timing requirements
4. Large size and number of loads

2-8. What is the basic storage element in a dynamic semiconductor memory cell?

1. A capacitor
2. A resistor
3. Magnetism
4. Reluctance

dynamic semiconductor memory is known as

1. replacing
2. purging
3. initialing
4. refreshing

IN ANSWERING QUESTIONS 2-10 AND 2-11 REFER TO FIGURE 1-32 AND THE APPROPRIATE IN YOUR RTM.

What is the storage element of this circuit?

1. Gate capacitance of Q_1
2. Gate capacitance of Q_2
3. Gate Capacitance of Q_3
4. Conduction state of the refresh amplifier

In reading data from the cell, what will be the result on the read bus voltage if a 0 is stored in the storage cell?

1. It will not be affected
2. It will be reduced to 0
3. It will assume the opposite value of the gate voltage of Q_2
4. It will not be reduced significantly

Learning Objective: Explain some features of the various types of read-only memories (ROMs).

Which of the following is the main distinguishing characteristic of a ROM?

1. It contains permanently stored binary information
2. It is designed to be a sequential access device
3. It contains semi-permanently stored digital information
4. Data can be written into it under program control

What is the primary application of a ROM in a digital computer?

1. Used as main memory for clocking circuits
2. Used in power supply high "Z" filter circuits
3. Used to perform digital-to-analog conversions
4. Used as main memory for storing programs and data

1. It is impervious to voltage transients
2. Its failure rate is very low
3. Its high speed
4. Its limited lead structure

IN ANSWERING QUESTIONS 2-15 THROUGH 2-17, SELECT THE DESCRIPTION IN COLUMN B THAT MATCHES THE DEVICE LISTED IN COLUMN A. NOT EVERY RESPONSE IN COLUMN B IS USED.

A. DEVICE

2-15. Mask ROM

2-16. PROM

2-17. EPROM

B. DESCRIPTION

1. Data stored in the memory can be erased and new information stored
2. Data must be known prior to manufacture and cannot be changed
3. Can be programmed in the field with a burner or blaster device
4. Programmed by application of a strong magnetic field

2-18. In a diode matrix ROM, what determines whether a 1 or a 0 is stored?

1. Polarity of the diode
2. Capacitance between the annode and cathodes
3. Presence or absence of a diode
4. Avalanche condition of the diode

2-19. What is the basic storage element in an MOS ROM?

1. MOS field effect transistor
2. Schottky diode
3. Magnetic core
4. Magnetic film

IN YOUR RTM.

2-20. What is Q_2?

1. A MOSFET switch
2. A storage element
3. A load resistance
4. An amplifier

Learning Objective: Describe how a digital computer communicates with external peripheral devices.

2-21. Which of the following is a function of the I/O section of a digital computer?

1. To perform logic level conversion
2. To act as a buffer in order to match the high-speed CPU to a low-speed peripheral unit
3. To act as an interface between the computer and any external devices
4. Each of the above

2-22. When multiple peripheral equipments are connected to a computer, what method is normally used to address the desired peripheral unit?

1. Acoustic selection
2. A binary word is used as an address
3. First-in/first-out method
4. Random sampling

Learning Objective: Describe and identify the methods used to transmit digital data.

2-23. What two methods are used to transmit digital data?

1. Slow and fast
2. In series and out of series
3. Serial and parallel
4. Linear and non-linear

main computer. If you discover that the transmission line consists of one interconnecting signal lead, what can you assume about the type of data transmission involved?

1. The cable is probably defective as more than one load is required
2. Serial data transmission is involved
3. Parallel data transmission is involved
4. Distributed transmission is involved

Learning Objective: Distinguish among the various causes of errors in the data transmission medium of a digital computer.

2-25. What should you do to reduce transmission line loss?

1. Use silicon cable connectors
2. Keep the transmission line as short as possible
3. Use high resistance cables
4. Use neoprene insulation on all conductors

2-26. Which of the following factors can cause distortion in digital data transmission lines?

1. Phase of the impedance compiled biasing current
2. Inductance and capacitance of the line
3. Phase shaft or delay introduced by a line
4. Both 2 and 3 above

Learning Objective: Identify and explain the purpose and use of line drivers and receivers.

linear distortion back into acceptable form
2. To reverse the long-term effects of logarithmic modulation
3. To act as the logic circuit that transmits the desired binary signals over certain types of transmission lines
4. To filter out modulation tones caused by distorted low level data bits

2-28. Which of the following is a function of a line receiver?

1. To generate logic signals compatible with the logic circuitry at the end of the line
2. To discriminate against any noise picked up on the line
3. To reshape the logic signal caused by line distortion
4. Each of the above

2-29. What characteristic of a Schmitt trigger circuit makes it desirable as a line receiver?

1. Its ability to pass low-level noise signals and transients
2. The logic states of the circuit will not change if the input signal passes through certain levels
3. Its built-in hysteresis and high noise immunity
4. Its ability to reject modulation tones caused by fiber optic lines

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Learning Objective: Identify and describe the two principal methods of data transmission.

2-30. Each bit of a binary word to be transmitted must have its own data path in what type of digital data transmission system?

1. Serial
2. Heterodyne
3. Parallel
4. Horizontal

2-31. What are the three basic types of double-wire transmission systems?

1. Coaxial, fiber, and parallel
2. Twisted pair, triaxial, and coaxial
3. Ribbon, romax, and parallel
4. Parallel, twisted pair, and coaxial

1. Faster response time
2. Greater rejection of noise
3. Flexibility
4. Transmission rate capability

2-33. Which of the following are disadvantages associated with coaxial cable?

1. High transmission loss and cost
2. Low noise immunity and impedance
3. Low noise immunity and complexity of construction
4. Absence of a shield and high transmission loss at the low end

2-34. In a balanced-line transmission system, how many inputs does the differential line receiver have?

1. One
2. Two
3. Three
4. Four

2-35. In a balanced-line transmission system, dual wire cable is used with (a) what type of frequencies and (b) at what distances?

1. (a) Intermediate (b) long
2. (a) High (b) long
3. (a) High (b) short
4. (a) Low (b) short

2-36. What method of digital data transmission is considered to be the simplest, most economical, and easiest to use?

1. Parallel
2. Serial
3. End around
4. Direct

2-37. Which of the following is an advantage realized from serial data transmission?

1. Low cost tape recorders can be used to record the data
2. Data can be transmitted over telephone wires
3. Data can be transmitted over long distances
4. Each of the above

TRANSMISSION DESCRIBED IN COLUMN A. NOT EVERY RESPONSE IN COLUMN B IS USED.

A. DESCRIPTION

2-38. Data can be transmitted in both directions simultaneously on the same transmission line

2-39. Data in a serial format is transmitted in one direction only

2-40. Data can be transmitted first in one direction and then the other, but cannot be transmitted in both directions at the same time

B. TRANSMISSION METHOD

1. Simplex
2. Complex
3. Half duplex
4. Full duplex

2-41. Start and stop pulses are used to mark the beginning and end of each data word transmitted in what type of serial data tranemission system?

1. Direct
2. Synchronous
3. Asynchronous
4. Insynchronous

2-42. The method of serial data transmission called frequency shift keying (FSK) uses what means to transmit binary data?

1. Audio tones
2. High frequency tones
3. Varying RF levels
4. Varying light frequencies

2-43. What type of unit is used to send and receive FSK serial data?

1. Encoder
2. Key generator
3. Matrix
4. Modem

2-44. What type of circuit can be used to transmit and receive serial data in a digital system?

1. CRT
2. UART
3. STD
4. NIXIE

1. Receiver
2. Transmitter
3. Detector
4. Controller

2-46. For most UARTs, the clock frequency is set to how many times the desired baud rate?

1. 1
2. 2
3. 3
4. 16

Learning Objective: Describe the concepts and procedures used in construction of a computer program.

2-47. A computer program that takes certain commands and translates them into instructions necessary for a computer to execute them is known as a

1. convertor
2. interpreter
3. translator
4. compiler

2-48. What is the purpose of a subroutine?

1. To store the entire program at various places in order to ensure reliability
2. To enter administrative data relative to program construction
3. To eliminate repeating certain groups of instructions throughout the program
4. To "delay" a program

2-49. What type of instructions control access to the various subroutines?

1. Operational routines
2. Executive routines
3. Selection routines
4. Access routines

2-50. Which of the following types of instructions provide the computer with the ability to leave the sequential execution of the main program, perform a subroutine, and then return to sequential execution?

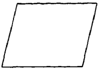
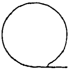
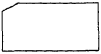
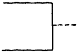
1. Sequencing instructions
2. Jump instructions
3. Return jump instructions
4. Both 2 and 3 above

FROM COLUMN B THE DESCRIPTION THAT
S THE PROCESS LISTED IN COLUMN A. NOT
SPONSES IN COLUMN B ARE USED.

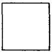
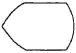
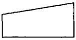
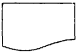
A. PROCESS	B. DESCRIPTION
Analysis	1. To locate errors in the program
Encoding	2. To use symbols to represent the various operations to be performed
Debugging	3. To layout the program in a form that will lend itself to interpretation
	4. To convert flow chart operations into computer language

Learning Objective: Recognize and define various flow chart symbols.

WERING QUESTIONS 2-54 THROUGH 2-58,
FROM COLUMN B THE FLOWCHART SYMBOL THAT
S THE DESCRIPTION IN COLUMN A. SYMBOLS
UMN B MAY BE USED MORE THAN ONCE.

A. DESCRIPTION	B. SYMBOL
Used as an annotation symbol	1. 
Used to represent an I/O function whose medium is punched cards	2. 
Used to represent an I/O function whose medium is magnetic tape	
Used to add descriptive comments or clarification notes	3. 
Used to represent any medium or data available for processing, or the processed information	4. 

represent an I/O function in which the information is to be displayed by means of video devices?

1. 
2. 
3. 
4. 

Learning Objective: Identify and define the various programs used in preventive and corrective maintenance of computers.

2-60. What means provides a thorough and rapid method for the detection of failures in a specific portion of a computer?

1. Analysis
2. A debugging check
3. A maintenance program
4. An error check

2-61. What type of maintenance programs are designed to detect the existence of errors?

1. Reliability programs
2. Subroutines
3. Utility programs
4. Executive routines

2-62. What type of maintenance program should you use to locate the circuits in which computer malfunctions originate?

1. Reliability programs
2. Locator programs
3. Diagnostic programs
4. Utility programs

detect circuit failures that occur only under particular operating conditions?

1. Detection
2. Reliability
3. Variable parameter
4. Discovery

2-64. Once a reliability program detects a trouble, what type of program should be used to isolate the source of trouble?

1. Operational program
2. Isolation program
3. Diagnostic program
4. Status program

IN ANSWERING QUESTIONS 2-65 THROUGH 2-69, SELECT FROM COLUMN B THE DIAGNOSTIC PROGRAM THAT MATCHES THE DESCRIPTION IN COLUMN A. ITEMS IN COLUMN B MAY BE USED MORE THAN ONCE.

A. DESCRIPTION	B. PROGRAM
2-65. Small number of circuits initially checked followed by successive addition of more circuits	1. Large area check 2. Overlapping area check
2-66. Large number of circuits initially checked followed by checks of smaller number of circuits if an error is detected	3. Increasing area check 4. Decreasing area check
2-67. Routines of this type of maintenance program overlap each other	
2-68. Used to detect the general area in which a malfunction occurs	
2-69. By this method, circuits which are found to be operating correctly are used to check other circuits	

maintenance programs from punched cards or magnetic tape into the computer memory section?

1. Reliability program
2. Diagnostic program
3. Maintenance program
4. Utility program

Assignment 3

ook Assignment: "IUSS Computers and Processors." Pages 2-1 through 2-56.

Learning Objective: Recognize the purpose and general characteristics of the AN/UYK-20 computer.

The AN/UYK-20 is used in computer applications requiring what type of data processing capability?

1. Small scale
2. Medium scale
3. Both 1 and 2 above
4. Large scale

The program stored in the main memory of the AN/UYK-20 consists of what type of instructions?

1. Miniinstructions
2. Microinstructions
3. Macroinstructions
4. Machoinstructions

What is the basic word length, in bits, of the AN/UYK-20?

1. 8
2. 16
3. 48
4. 4

What is the memory addressing capability of the AN/UYK-20?

1. 26K
2. 32K
3. 65K
4. 76K

What type of option adds square root, floating point, and trigonometric capabilities to the AN/UYK-20?

1. Mathpack
2. Extended AMI
3. 32 general registers
4. DDMF

Learning Objective: Identify the general characteristics of the Processor/IOC, memory chassis, and controls and indicators of the AN/UYK-20 computer.

3-6. The processor/IOC chassis contains what size of printed circuit cards?

1. Single- and double-width
2. Single- and triple-width
3. Double- and triple-width
4. Single-, double-, and triple-width

3-7. On the circuit cards contained in the processor/IOC, what is used to indicate the location of the first test point (TP1)?

1. A color code
2. A square blivet
3. The rightmost test point when the card is properly mounted
4. Both 2 and 3 above

3-8. The I/O connectors are keyed so input cables cannot be interchanged with output cables.

1. True
2. False

3-9. What is the capacity of each memory array broad?

1. 4K x 16
2. 8K x 16
3. 16K x 16
4. 32K x 16

memory controls boards and (b) memory data boards?

1. (a) One (b) one
2. (a) One (b) two
3. (a) Two (b) one
4. (a) Two (b) two

IN ANSWERING QUESTIONS 3-11 THROUGH 3-13, SELECT FROM COLUMN B THE FUNCTION THAT IS PERFORMED BY THE SWITCH LISTED IN COLUMN A. NOT EVERY RESPONSE IN COLUMN B IS USED.

	A. SWITCH		B. FUNCTION
3-11.	BLOWER POWER (S8)	1.	ON position disables the overtemperature shutdown function
3-12.	LOGIC POWER (S7)	2.	ON position enables primary power to the DPS
3-13.	BATTLE SHORT (S1)	3.	ON position enables the LOGIC POWER ON/OFF switch function
		4.	OFF position disables power to the dc power supply

Learning Objective: Display knowledge of programming instructions and formats.

3-14. In computer programming, which of the following definitions defines a repertoire?

1. Individual instruction words that perform relatively simple tasks
2. A group of instructions that perform a complex function
3. The instructions contained in a specific memory location
4. The array of instructions which allow a computer to function

many basic formats?

1. Five
2. Seven
3. Three
4. Four

IN ANSWERING QUESTIONS 3-16 THROUGH 3-20 SELECT FROM COLUMN B THE FORMAT THAT IS DESCRIBED IN COLUMN A. RESPONSES MAY BE USED MORE THAN ONCE.

	A. INSTRUCTION		B. FORMAT
3-16.	In this format a number in a register is to be added to a number in a register	1.	RK
3-17.	In this format one operand is in a register and the other is in main memory	2.	RX
3-18.	Allows the instruction word to define a constant	3.	RR
3-19.	Performs operations such as data shifts	4.	RL
3-20.	Is the most versatile format in the repetoire and will facilitate a variety of operations		

3-21. Computer registers whose contents can be changed by a program, or by an instruction being executed, are known by which of the following names?

1. Accumulator registers
2. Addressable registers
3. General registers
4. Both 2 and 3 above

3-22. Which of the following instruction word formats are 32 bits in length?

1. RR and RI
2. RI and RR
3. RL and RI
4. RK and RX

The op code field in an AN/UYK-20 can contain what maximum value?

1. 77_8
2. 100_8
3. 120_8
4. 177_8

4. What is contained in the "P" register?

1. Instructions
2. Address words
3. Data words
4. Operands

5. If a double-length data word is in two consecutive memory locations, which of the following statements regarding the memory addresses of the most significant 16 bits is correct?

1. They are located in the lower numbered address and the lower numbered address must be odd
2. They are located in the higher numbered address and the higher numbered address must be odd
3. They are located in the lower numbered address and the lower numbered address must be even
4. They are located in either the upper or lower numbered address, however, the lower numbered address must be even

6. In the AN/UYK-20, how many bits are there in a byte?

1. 8
2. 16
3. 32
4. 4

7. In a literal data type word, where, if at all, is the sign bit located?

1. Bit position 03
2. Bit position 02
3. Bit position 00
4. A sign bit is not used

3. What type of instruction is used to move data from one area of the AN/UYK-20 to another?

1. Data transfer
2. Jump
3. Logic and Shift
4. I/O

3-29. What are the two types of jump instructions?

1. Conditional and arbitrary
2. Transfer and return
3. Conditional and unconditional
4. Destructive and nondestructive

3-30. An instruction that is very similar to a data transfer except that a mathmetical operation is performed, is known by what name?

1. Logic
2. Jump
3. Arithmetic
4. Retard

3-31. What type of instructions are used to control information flow into or out of the AN/UYK-20?

1. Miscellaneous
2. I/O and interrupt control
3. Arithmetic
4. Jump

Learning Objective: State the function of the Microprogram Controller (MPC) and determine how many microinstructions it can execute.

3-32. What is the function of the MPC?

1. It performs arithmetic and data transfer functions as directed by the macroinstructions
2. It stores the majority of the macroinstructions for data manipulation
3. It provides all control functions that enable the computer to execute the program stored in main memory
4. It controls the rate of data transfer between the I/O and peripheral equipments

3-33. The MPC can execute how many basic microinstructions?

1. 16
2. 32
3. 64
4. 4

Learning Objective: Identify the components of the MPC and some of their functions and characteristics.

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memory?

1. 8K
2. 2K
3. 12K
4. 4K

3-35. What section of the MPC contains the master clock?

1. Micro memory control
2. Micro function control
3. Arithmetic logic
4. Micro memory

3-36. What section of the MPC provides the interface between the maintenance panel and the displayable registers of the DPS?

1. Processor/emulator
2. Repeat control
3. Arithmetic/logic
4. Display control

3-37. What section contains logic circuits that augment the MPC?

1. Processor/emulator
2. Micro memory
3. Micro function control
4. Repeat control

3-38. When two sets of general registers are used, what determines which general register set is addressed?

1. Bit 16 of the general register address
2. A status register bit
3. An accumulator register bit
4. An I/O address bit

3-39. What section of the MPC contains the two status registers?

1. Memory status
2. Program status
3. High-speed shift and multiply
4. Memory interface

3-40. What section of the MPC handles the transfer of information between the processor/emulator and main memory, and between the I/O controller and main memory?

1. Program status
2. I/O controller
3. I/O interface
4. Memory interface

memory of the AN/UYK-20.

1. True
2. False

3-42. The I/O controller of the MPC allows for interface between the AN/UYK-20 and a maximum of how many peripheral units?

1. 14
2. 15
3. 16
4. 17

3-43. Serial and parallel channels of the I/O controller can be combined in any combination up to the maximum capacity as long as they are provided in how many groups for (a) parallel and (b) serial?

1. (a) Two (b) two or four
2. (a) Two (b) one or two
3. (a) Four (b) two or four
4. (a) Four (b) one or two

IN ANSWERING QUESTIONS 3-44 THROUGH 3-46, SELECT FROM COLUMN B THE FUNCTION PERFORMED BY THE PARALLEL INTERFACE LISTED IN COLUMN A. NOT EVERY RESPONSE IN COLUMN B IS USED.

A. INTERFACE

3-44. NTDS Slow

3-45. NTDS Fast

3-46. ANEW

B. FUNCTION

1. 0V to represent binary 1 and -3V to represent binary 0
2. 0V to represent binary 1 and -15V to represent binary 0
3. 0V to represent binary 1 and -15V to represent binary 0
4. +6V to represent ON and -6V to represent OFF

HE SERIAL INTERFACE LISTED IN COLUMN A. NOT
VERY RESPONSE IN COLUMN B IS USED.

A. INTERFACE	B. FUNCTION
-47. MILSTD 188C	1. +3V ON and -12V OFF for binary 0 and binary 1, respectively
-48. VACALES	2. Operates in asynchronous mode and uses 32-bit data transfer
-49. NTDS 32-bit serial	3. Provides four independent, full duplex, synchronous serisl channels
	4. Seven discrete lines with +6V ON and -6V OFF

Learning Objective: Display knowledge of the maintenance concepts of the AN/UYK-20

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50. What is the primary maintenance tool used in support of the AN/UYK-20 computer?

1. AN/PSM-1A
2. ZM-11U
3. Diagnostic routines
4. SWAGs

51. The program fault indicators on the AN/UYK-20 are capable of detecting a malfunction in what major element of the computer?

1. Software only
2. Hardware only
3. Either software or hardware

following troubleshooting methods should be taken?

1. Use of flow diagrams and lamp and relsy indexes
2. Use of OP stsp or micro step modes
3. Csrd swapping
4. Each of the above

Learning Objective: Identify the general characteristics and components of the Synchronous Distributed Processor (SDP).

3-53. Which of the following features of the SDP makes it suitable for a wide range of applications?

1. It includes all hardware, software, training aids, and documentstion
2. It is highly programmable
3. It sllows for multiple configurations
4. Each of the above

IN ANSWERING QUESTIONS 3-54 THROUGH 3-56, SELECT THE FUNCTION IN COLUMN B THAT IS PERFORMED BY THE SDP COMPONENT LISTED IN COLUMN A. NOT EVERY RESPONSE IN COLUMN B IS USED.

A. COMPONENT	B. FUNCTION
3-54. Processor Module	1. Provides for system control functions
3-55. Interface/Memory Module	2. Psrforms IAU, AU, and IOU functions
3-56. Satellite Processor Unit	3. Contains IAU/AU operand and IOU buffer memory
	4. Provides power distribution and overcurrent protection

additional multiplexers?

1. 5
2. 15
3. 30
4. 45

3-58. How many parallel microprocessors are contained in each processor module?

1. Five
2. Two
3. Three
4. Four

3-59. What is the clock rate for each module of the SDP?

1. 8 MHz
2. 16 MHz
3. 24 MHz
4. 5 MHz

3-60. From where does the SPU obtain its boot program after power is applied?

1. From an EPROM card in the SPU
2. From a disk drive system
3. From a Kennedy 9000 tape drive
4. From an EPROM card in the IMM

3-61. What portion of the SPU program detects the boot conditions of the SDP and issues commands to boot the SDP programs?

1. Fault table
2. Error detector
3. Localizer
4. PM/FL

3-62. What is the function of the lower 16-position thumb wheel switch of the test and monitor panel of the PM?

1. To call up displays to the REGISTER CONTENT indicators
2. To transmit information to the IAU status register when the transmit information SENSE LOAD switch is depressed
3. To clear corresponding memory blocks from the IMM when MASTER CLEAR is activated
4. To test I/O parts associated with the switch number when the RUN switch is activated

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Learning Objective: Demonstrate familiarity with the basic operating procedures of the Synchronous Distributed Processor (SDP).

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1. When there is loss of software control
2. When system operation with a degraded SPU is required and for testing purposes
3. When realignment of all clock frequencies is necessary
4. When there is a momentary power loss

3-64. Remote alarms are activated when power is removed from the SDP. How should you disable the remote alarms?

1. By placing the NORMAL MAINT switch to the MAINT position
2. By placing the NORMAL MAINT switch to the NORMAL position
3. By removing the 6.3Vac fuse
4. By unplugging the cabinet from the power strip

Learning Objective: Describe the difference between the two Satellite Processor Units (SPUs) available and identify some characteristics of their internal memory management systems.

3-65. What is the primary difference between the LSI-11/2 and LSI-11/23 microprocessors?

1. The LSI-11/23 has twice the memory capacity of the LSI-11/2
2. The memory management nest and memory control/processor are not present in the LSI-11/2, but are in the LSI-11/23
3. The memory management nest and memory control/processor are not present in the LSI-11/23, but are in the LSI-11/2
4. The LSI-11/23 has a memory cycle time of 38 nsec while on the LSI-11/2 it is 42 nsec

3-66. In the SPU, what is the interfacing characteristic of the DLV11-J?

1. Three-channel synchronous
2. Four-channel synchronous
3. Four-channel asynchronous
4. Four-channel multiplexed

1. DLV11-J
2. DRV11
3. MSV11-DD
4. MRV11-BA

8. How many words of static RAM are contained in the MRV11-BA UV EPROM/RAM MEMORY card of the SPU?

1. 4K
2. 32K
3. 570
4. 256

9. How many MCBs are included in the SPU (LSI-11/2)?

1. One
2. Two
3. Three
4. Four

0. A clock signal is provided to the SPU by the line time clock in the form of an interrupt at what frequency rate?

1. 60 Hz
2. 2 kHz
3. 12 kHz
4. 4 kHz

Learning Objective: Identify the units which comprise the Processor Module (PM) of the SDP and describe their functions.

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1. IAU, AU, and IOU
2. SDP, PM, and IAU
3. SPU, IAU, and I/O
4. I/O, RU, and IAU

3-72. What is the function of the IAU of the PM?

1. To perform arithmetic and logic operations on the data inputs
2. To serve as the interface between the AU and IOU
3. To exercise overall algorithm control and generate addresses for the working memory
4. To control all I/O operations from the SDP cabinet

3-73. What section of the IAU of the PM holds data for sequencing the program and generating working memory addresses?

1. Cyclic array addressing
2. IAU program memory
3. Sequence microprocessor
4. Index memory

3-74. How many machine cycles are required for the AU of the PM to perform a multiply operation?

1. One
2. Two
3. Three
4. Four

3-75. The principal task of queuing data for the input and output is performed by what section of the PM?

1. IAU
2. IOU
3. IOM
4. AU

Assignment 4

Textbook Assignment: "IUSS Computers and Processors" (continued) and "Peripheral Equipment."
Pages 2-59 through 3-40.

Learning Objective: Identify the general types and characteristics of the memories in the Interface Memory Module (IMM) of the SDP.

4-1. What SDP module incorporates the working and I/O buffer memory systems?

1. PM
2. UM
3. SPU
4. IMM

4-2. The read and write data paths out of and into buffer memory are how many bits wide?

1. 17
2. 20
3. 21
4. 24

4-3. What is the maximum static memory configuration for an IMM?

1. One 16K RAM
2. One 65K RAM
3. Sixteen 65K cards
4. Sixty-four 16K cards

4-4. What is the minimum dynamic memory configuration for an IMM?

1. One controller and one 16K RAM
2. One controller and sixty-four 16K RAMs
3. One controller and one 65K RAM
4. One controller and sixteen 65K RAMs

4-5. How is portioning accomplished in setting up the various parameters of an IMM?

1. By cutting various ribbon cables
2. By removing groups of cards
3. By changing the EPROMs
4. By expanding the IMM configuration

Learning Objective: Describe how the AN/UYK-7 computer interfaces with other units.

4-6. On the AN/UYK-7 computer, how does the central processor (CP) interface with the memory units?

1. Via the disk drive
2. Via the IOC
3. Via an I/O bus
4. Via the IPU

4-7. Each CP can address the equivalent of up to (a) how many core memory units and control (b) how many I/O controllers?

1. (a) 16 (b) 4
2. (a) 12 (b) 4
3. (a) 8 (b) 2
4. (a) 4 (b) 2

4-8. How does the I/O controller interface with external devices?

1. Through the IOC
2. Through the I/O adapter
3. Through IPU
4. Through memory units

4-9. How are data transfers between units of the AN/UYK-7 handled?

1. On a synchronous basis
2. On an asynchronous basis
3. They are multiplexed
4. They are modulated

Learning Objective: Identify the types of memory used on the AN/UYK-7 computer.

type of memory?

1. DRO
2. NDRO
3. ADRO
4. RO

1. The control memory contains how many flip-flop storage registers?

1. 16
2. 32
3. 54
4. 82

2. What is the purpose of NDRO memories?

1. To provide a storage residence for macroinstructions associated with data transfers
2. To store data used for operand address modification and interrupt execution
3. To provide a means of automatically loading the DRO memory, and to provide for hardware fault analysis and load-failure analysis programs
4. To provide for monitor clock update operations

. How many NDRO memories are required for each type of peripheral equipment and I/O channel used?

1. One
2. Two
3. Three
4. Four

Learning Objective: Identify the basic operating characteristics of the AN/UYK-7 computer.

. What part of the AN/UYK-7 controls the overall operation of the computer?

1. The CP
2. The IOC
3. The IOA
4. The memory units

. The CP obtains instructions from the memory units via what bus?

1. I
2. O
3. A
4. C

does the chassis side cover and ribbed heat exchanger plate of the CP provide?

1. Structural integrity
2. AF shielding
3. RF shielding
4. LF shielding

4-17. The I/O controller interfaces with peripheral equipments via what device?

1. I/O keyer
2. I/O modulator
3. I/O matcher
4. I/O adapter

4-18. How many I/O channels are contained on the I/O adapter?

1. 16
2. 32
3. 64
4. 4

4-19. On the AN/UYK-7, what is the memory capacity of a core memory unit?

1. 8K
2. 16K
3. 32K
4. 4K

4-20. What is the maximum addressable memory for the AN/UYK-7 computer with one CP?

1. 200K
2. 262K
3. 362K
4. 524K

4-21. If power to the AN/UYK-7 fails, the computer will be supplied stored power for what maximum length of time?

1. 250 microseconds
2. 250 nanoseconds
3. 250 milliseconds
4. 250 megaseconds

4-22. You should apply dc power to the maintenance console from what unit on the AN/UYK-7?

1. Operator panel
2. Remote console
3. Auxiliary control
4. Maintenance console

Learning Objective: Describe the general operational characteristics of the Super Bee computer terminal.

4-23. What type of format is used by the Super Bee II to receive and transmit data?

1. Serial
2. Parallel
3. Forced
4. Multiplexed

4-24. The Super Bee II can display a maximum of how many characters per line?

1. 25
2. 35
3. 80
4. 120

4-25. Following a change from the HDX to FDX mode, what key must also be pressed?

1. CLEAR
2. RESET
3. ENTER
4. ESC

4-26. What transmission mode is generally used to transmit precomposed messages either a few lines at a time or as an entire memory dump?

1. Multiplex
2. Echoplex
3. Half duplex
4. Full duplex

4-27. What is the fastest baud rate possible with a Super Bee II unit with 10-bit word operation?

1. 2400
2. 3520
3. 7040
4. 9600

4-28. What maximum number of characters can be displayed at any one time on the Super Bee II computer terminal?

1. 5K
2. 2K
3. 3K
4. 4K

4-29. If you perform a clear operation by preesing the CLEAR key on the keyboard of the Super Bee computer terminal, which of the following actions will result?

1. Memory will be filled with space codes
2. Cursor will be positioned to the home position
3. Data in memory will be irradicated
4. All the above

Learning Objective: Identify some aspects of the seven major functional components of the Super Bee computer terminal.

4-30. What voltage levels and polarity are provided by the power supply unit?

1. +5, -15, -12 V dc
2. +5, +15, -12 V dc
3. -5, +15, +12 V dc
4. -5, -15, +12 V dc

4-31. The video brightness control is contained on what part of the Super Bee unit?

1. Back of the console
2. Side of the console
3. Keyboard
4. I/O board

4-32. What is the ASCII code for the letter E?

1. 1000101
2. 0101100
3. 1010100
4. 1001010

4-33. What is the source of the vertical, horizontal, and video output signals used by the monitor assembly?

1. Deflection yoke
2. Interconnect board
3. Display board
4. I/O board

4-34. How many banks of shift registers are contained in the page memory portion of the display board?

1. Eight
2. Two
3. Six
4. Four

The OP code field in an AN/UYK-20 can contain what maximum value?

1. 77_8
2. 100_8
3. 120_8
4. 177_8

What is contained in the "P" register?

1. Instructions
2. Address words
3. Data words
4. Operands

If a double-length data word is in two consecutive memory locations, which of the following statements regarding the memory addresses of the most significant 16 bits is correct?

1. They are located in the lower numbered address and the lower numbered address must be odd
2. They are located in the higher numbered address and the higher numbered address must be odd
3. They are located in the lower numbered address and the lower numbered address must be even
4. They are located in either the upper or lower numbered address, however, the lower numbered address must be even

In the AN/UYK-20, how many bits are there in a byte?

1. 8
2. 16
3. 32
4. 4

In a literal data type word, where, if at all, is the sign bit located?

1. Bit position 03
2. Bit position 02
3. Bit position 00
4. A sign bit is not used

What type of instruction is used to move data from one area of the AN/UYK-20 to another?

1. Data transfer
2. Jump
3. Logic and Shift
4. I/O

3-29. What are the two types of jump instructions?

1. Conditional and arbitrary
2. Transfer and return
3. Conditional and unconditional
4. Destructive and nondestructive

3-30. An instruction that is very similar to a data transfer except that a mathmetical operation is performed, is known by what name?

1. Logic
2. Jump
3. Arithmetic
4. Retard

3-31. What type of instructions are used to control information flow into or out of the AN/UYK-20?

1. Miscellaneous
2. I/O and interrupt control
3. Arithmetic
4. Jump

Learning Objective: State the function of the Microprogram Controller (MPC) and determine how many microinstructions it can execute.

3-32. What is the function of the MPC?

1. It performs arithmetic and data transfer functions as directed by the macroinstructions
2. It stores the majority of the macroinstructions for data manipulation
3. It provides all control functions that enable the computer to execute the program stored in main memory
4. It controls the rate of data transfer between the I/O and peripheral equipments

3-33. The MPC can execute how many basic microinstructions?

1. 16
2. 32
3. 64
4. 4

Learning Objective: Identify the components of the MPC and some of their functions and characteristics.

---

memory?

1. 8K
2. 2K
3. 12K
4. 4K

3-35. What section of the MPC contains the master clock?

1. Micro memory control
2. Micro function control
3. Arithmetic logic
4. Micro memory

3-36. What section of the MPC provides the interface between the maintenance panel and the displayable registers of the DPS?

1. Processor/emulator
2. Repeat control
3. Arithmetic/logic
4. Display control

3-37. What section contains logic circuits that augment the MPC?

1. Processor/emulator
2. Micro memory
3. Micro function control
4. Repeat control

3-38. When two sets of general registers are used, what determines which general register set is addressed?

1. Bit 16 of the general register address
2. A status register bit
3. An accumulator register bit
4. An I/O address bit

3-39. What section of the MPC contains the two status registers?

1. Memory status
2. Program status
3. High-speed shift and multiply
4. Memory interface

3-40. What section of the MPC handles the transfer of information between the processor/emulator and main memory, and between the I/O controller and main memory?

1. Program status
2. I/O controller
3. I/O interface
4. Memory interface

transfers data to and from the main memory of the AN/UYK-20.

1. True
2. False

3-42. The I/O controller of the MPC allows for interface between the AN/UYK-20 and a maximum of how many peripheral units?

1. 14
2. 15
3. 16
4. 17

3-43. Serial and parallel channels of the I/O controller can be combined in any combination up to the maximum capacity as long as they are provided in how many groups for (a) parallel and (b) serial?

1. (a) Two (b) two or four
2. (a) Two (b) one or two
3. (a) Four (b) two or four
4. (a) Four (b) one or two

IN ANSWERING QUESTIONS 3-44 THROUGH 3-46, SELECT FROM COLUMN B THE FUNCTION PERFORMED BY THE PARALLEL INTERFACE LISTED IN COLUMN A. NOT EVERY RESPONSE IN COLUMN B IS USED.

A. INTERFACE

3-44. NTDS Slow

3-45. NTDS Fast

3-46. ANEW

B. FUNCTION

1. 0V to represent binary 1 and -3V to represent binary 0
2. 0V to represent binary 1 and -15V to represent binary 0
3. 0V to represent binary 1 and -15V to represent binary 0
4. +6V to represent ON and -6V to represent OFF

ERIAL INTERFACE LISTED IN COLUMN A. NOT
RESPONSE IN COLUMN B IS USED.

A. INTERFACE	B. FUNCTION
MILSTD 188C	1. +3V ON and -12V OFF for binary 0 and binary 1, respectively
VACALES	2. Operates in asynchronous mode and uses 32-bit data transfer
NTDS 32-bit serial	3. Provides four independent, full duplex, synchronous serial channels
	4. Seven discrete lines with +6V ON and -6V OFF

Learning Objective: Display knowledge of the maintenance concepts of the AN/UYK-20

What is the primary maintenance tool used in support of the AN/UYK-20 computer?

1. AN/PSM-1A
2. ZM-11U
3. Diagnostic routines
4. SWAGs

The program fault indicators on the AN/UYK-20 are capable of detecting a malfunction in what major element of the computer?

1. Software only
2. Hardware only
3. Either software or hardware

following troubleshooting methods should be taken?

1. Use of flow diagrams and lamp and relay indexes
2. Use of OP step or micro step modes
3. Card swapping
4. Each of the above

Learning Objective: Identify the general characteristics and components of the Synchronous Distributed Processor (SDP).

3-53. Which of the following features of the SDP makes it suitable for a wide range of applications?

1. It includes all hardware, software, training aids, and documentation
2. It is highly programmable
3. It allows for multiple configurations
4. Each of the above

IN ANSWERING QUESTIONS 3-54 THROUGH 3-56, SELECT THE FUNCTION IN COLUMN B THAT IS PERFORMED BY THE SDP COMPONENT LISTED IN COLUMN A. NOT EVERY RESPONSE IN COLUMN B IS USED.

A. COMPONENT	B. FUNCTION
3-54. Processor Module	1. Provides for system control functions
3-55. Interface/Memory Module	2. Performs IAU, AU, and IOU functions
3-56. Satellite Processor Unit	3. Contains IAU/AU operand and IOU buffer memory
	4. Provides power distribution and overcurrent protection

additional multiplexers?

1. 5
2. 15
3. 30
4. 45

3-58. How many parallel microprocessors are contained in each processor module?

1. Five
2. Two
3. Three
4. Four

3-59. What is the clock rate for each module of the SDP?

1. 8 MHz
2. 16 MHz
3. 24 MHz
4. 5 MHz

3-60. From where does the SPU obtain its boot program after power is applied?

1. From an EPROM card in the SPU
2. From a disk drive system
3. From a Kennedy 9000 tape drive
4. From an EPROM card in the IMM

3-61. What portion of the SPU program detects the boot conditions of the SDP and issues commands to boot the SDP programs?

1. Fault table
2. Error detector
3. Localizer
4. PM/FL

3-62. What is the function of the lower 16-position thumb wheel switch of the test and monitor panel of the PM?

1. To call up displays to the REGISTER CONTENT indicators
2. To transmit information to the IAU status register when the transmit information SENSE LOAD switch is depressed
3. To clear corresponding memory blocks from the IMM when MASTER CLEAR is activated
4. To test I/O parts associated with the switch number when the RUN switch is activated

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Learning Objective: Demonstrate familiarity with the basic operating procedures of the Synchronous Distributed Processor (SDP).

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1. When there is loss of software control
2. When system operation with a degraded SPU is required and for testing purposes
3. When realignment of all clock frequencies is necessary
4. When there is a momentary power loss

3-64. Remote alarms are activated when power is removed from the SDP. How should you disable the remote alarms?

1. By placing the NORMAL MAINT switch to the MAINT position
2. By placing the NORMAL MAINT switch to the NORMAL position
3. By removing the 6.3Vac fuse
4. By unplugging the cabinet from the power strip

Learning Objective: Describe the difference between the two Satellite Processor Units (SPUs) available and identify some characteristics of their internal memory management systems.

3-65. What is the primary difference between the LSI-11/2 and LSI-11/23 microprocessors?

1. The LSI-11/23 has twice the memory capacity of the LSI-11/2
2. The memory management nest and memory control/processor are not present in the LSI-11/2, but are in the LSI-11/23
3. The memory management nest and memory control/processor are not present in the LSI-11/23, but are in the LSI-11/2
4. The LSI-11/23 has a memory cycle time of 38 nsec while on the LSI-11/2 it is 42 nsec

3-66. In the SPU, what is the interfacing characteristic of the DLV11-J?

1. Three-channel synchronous
2. Four-channel synchronous
3. Four-channel asynchronous
4. Four-channel multiplexed

1. DLV11-J
2. DRV11
3. MSV11-DD
4. MRV11-BA

3-68. How many words of static RAM are contained in the MRV11-BA UV EPROM/RAM MEMORY card of the SPU?

1. 4K
2. 32K
3. 570
4. 256

3-69. How many MCBs are included in the SPU (LSI-11/2)?

1. One
2. Two
3. Three
4. Four

3-70. A clock signal is provided to the SPU by the line time clock in the form of an interrupt at what frequency rate?

1. 60 Hz
2. 2 kHz
3. 12 kHz
4. 4 kHz

Learning Objective: Identify the units which comprise the Processor Module (PM) of the SDP and describe their functions.

---

1. IAU, AU, and IOU
2. SDP, PM, and IAU
3. SPU, IAU, and I/O
4. I/O, RU, and IAU

3-72. What is the function of the IAU of the PM?

1. To perform arithmetic and logic operations on the data inputs
2. To serve as the interface between the AU and IOU
3. To exercise overall algorithm control and generate addresses for the working memory
4. To control all I/O operations from the SDP cabinet

3-73. What section of the IAU of the PM holds data for sequencing the program and generating working memory addresses?

1. Cyclic array addressing
2. IAU program memory
3. Sequence microprocessor
4. Index memory

3-74. How many machine cycles are required for the AU of the PM to perform a multiply operation?

1. One
2. Two
3. Three
4. Four

3-75. The principal task of queuing data for the input and output is performed by what section of the PM?

1. IAU
2. IOU
3. IOM
4. AU

Assignment 4

Textbook Assignment: "IUSS Computers and Processors" (continued) and "Peripheral Equipment." Pages 2-59 through 3-40.

Learning Objective: Identify the general types and characteristics of the memories in the Interface Memory Module (IMM) of the SDP.

4-1. What SDP module incorporates the working and I/O buffer memory systems?

1. PM
2. UM
3. SPU
4. IMM

4-2. The read and write data paths out of and into buffer memory are how many bits wide?

1. 17
2. 20
3. 21
4. 24

4-3. What is the maximum static memory configuration for an IMM?

1. One 16K RAM
2. One 65K RAM
3. Sixteen 65K cards
4. Sixty-four 16K cards

4-4. What is the minimum dynamic memory configuration for an IMM?

1. One controller and one 16K RAM
2. One controller and sixty-four 16K RAMs
3. One controller and one 65K RAM
4. One controller and sixteen 65K RAMs

4-5. How is portioning accomplished in setting up the various parameters of an IMM?

1. By cutting various ribbon cables
2. By removing groups of cards
3. By changing the EPROMs
4. By expanding the IMM configuration

Learning Objective: Describe how the AN/UYK-7 computer interfaces with other units.

4-6. On the AN/UYK-7 computer, how does the central processor (CP) interface with the memory units?

1. Via the disk drive
2. Via the IOC
3. Via an I/O bus
4. Via the IPU

4-7. Each CP can address the equivalent of up to (a) how many core memory units and control (b) how many I/O controllers?

1. (a) 16 (b) 4
2. (a) 12 (b) 4
3. (a) 8 (b) 2
4. (a) 4 (b) 2

4-8. How does the I/O controller interface with external devices?

1. Through the IOC
2. Through the I/O adapter
3. Through IPU
4. Through memory units

4-9. How are data transfers between units of the AN/UYK-7 handled?

1. On a synchronous basis
2. On an asynchronous basis
3. They are multiplexed
4. They are modulated

Learning Objective: Identify the types of memory used on the AN/UYK-7 computer.

type of memory?

1. DRO
2. NDRO
3. ADRO
4. RO

11. The control memory contains how many flip-flop storage registers?

1. 16
2. 32
3. 54
4. 82

12. What is the purpose of NDRO memories?

1. To provide a storage residence for macroinstructions associated with data transfers
2. To store data used for operand address modification and interrupt execution
3. To provide a means of automatically loading the DRO memory, and to provide for hardware fault analysis and load-failure analysis programs
4. To provide for monitor clock update operations

13. How many NDRO memories are required for each type of peripheral equipment and I/O channel used?

1. One
2. Two
3. Three
4. Four

Learning Objective: Identify the basic operating characteristics of the AN/UYK-7 computer.

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14. What part of the AN/UYK-7 controls the overall operation of the computer?

1. The CP
2. The IOC
3. The IOA
4. The memory units

15. The CP obtains instructions from the memory units via what bus?

1. I
2. O
3. A
4. C

does the chassis side cover and ribbed heat exchanger plate of the CP provide?

1. Structural integrity
2. AF shielding
3. RF shielding
4. LF shielding

4-17. The I/O controller interfaces with peripheral equipments via what device?

1. I/O keyer
2. I/O modulator
3. I/O matcher
4. I/O adapter

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Learning Objective: Describe the general operational characteristics of the Super Bee computer terminal.

4-23. What type of format is used by the Super Bee II to receive and transmit data?

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3. 3K
4. 4K

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4. All the above

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1. Eight
2. Two
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ME ______________________________ ADDRESS ______________________________
Last First Middle Street/Ship/Unit/Division, etc.

City or FPO State Zip
NK/RATE ________ SOC. SEC. NO. ________________ DESIGNATOR ________ ASSIGNMENT NO. ________
☐ USN ☐ USNR ☐ ACTIVE ☐ INACTIVE OTHER (Specify) ________________ DATE MAILED ________

SCORE

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City or FPO State Zip

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NAME ______________________________ ADDRESS ______________________________
Last First Middle Street/Ship/Unit/Division, etc.

City or FPO State Zip

RANK/RATE ________ SOC. SEC. NO. ____________________ DESIGNATOR ________ ASSIGNMENT NO. ________

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NAME ______________________ ADDRESS ______________________
Last First Middle Street/Ship/Unit/Division, etc.

City or FPO State Zip

RANK/RATE ________ SOC. SEC. NO. ________________ DESIGNATOR ________ ASSIGNMENT NO. ________

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NAME ______________________________ ADDRESS ______________________________
Last First Middle Street/Ship/Unit/Division, etc.

City or FPO State Zip

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Last First Middle

Street/Ship/Unit/Division, etc.

City or FPO State Zip

RANK/RATE ________ SOC. SEC. NO. ______________________ DESIGNATOR ________ ASSIGNMENT NO. ________

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Last First Middle Street/Ship/Unit/Division, etc.

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City or FPO State Zip

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